POLITECHNIKA LUBELSKA

Profesor

Gopakumar Kumarukuttan Nair

Doktor Honoris Causa
Politechniki Lubelskiej

Lublin 2022

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POLITECHNIKA
LUBELSKA
WYDAWNICTWO

Lublin 2022

POLITECHNIKA
LUBELSKA
WYDZIAŁ ELEKTROTECHNIKI
I INFORMATYKI

Publikacja wydana za zgodą Rektora Politechniki Lubelskiej

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Uchwała Nr 14/2020/III
Senatu Politechniki Lubelskiej
z dnia 12 marca 2020 r.

w sprawie nadania
prof. Gopakumar Kumarukuttan Nair
tytułu doktora honoris causa Politechniki Lubelskiej

Działając zgodnie z § 23 ust. 1 pkt 2 oraz § 7 ust. 2 Statutu Politechniki Lubelskiej, na wniosek Rady Dyscypliny Naukowej Automatyka, Elektronika i Elektrotechnika Politechniki Lubelskiej, Senat u c h w a l a, co następuje:

§ 1.

Senat Politechniki Lubelskiej, po zapoznaniu się z opiniami prof. Leopoldo Garcia Franquelo z University of Seville (Spain), prof. Joachima Holtza z University of Wuppertal (Germany) i prof. dr. hab. inż. Mariana P. Kaźmierkowskiego z Politechniki Warszawskiej, oceniając dorobek naukowy, dydaktyczny i organizacyjny jako wybitny

n a d a j e

prof. Gopakumar Kumarukuttan Nair

tytuł

DOKTORA HONORIS CAUSA
POLITECHNIKI LUBELSKIEJ

§ 2.

Uchwała wchodzi w życie z dniem podpisania przez rektora Politechniki Lubelskiej.

Przewodniczący
Senatu Politechniki Lubelskiej

R e k t o r
Prof. dr hab. inż. Piotr Kacejko

SUMMIS AUSPICIIS
SERENISSIMAE REI PUBLICAE POLONORUM
NOS
RECTOR ET SENATUS POLYTECHNICAE LUBLINENSIS
ET
DECANUS FACULTATIS ELECTROTECHNICAE ET INFORMATICAE
NEC NON
PROMOTOR RITE CONSTITUTUS
CUM
UNANIMO CONSENSU SENATUUM
POLYTECHNICAE VARSOVIENSIS, UNIVERSITATIS HISPALENSIS, UNIVERSITATIS VALLIS VIPPERAE

IN
CLARISSIMUM ET DOCTISSIMUM PROFESSOREM
ARTIS ELECTRONICAE ENERGIAE PERITISSIMUM

GOPAKUMAR KUMARUKUTTAN NAIR

QUI GRAVEM GRANDEMQUE IN ORBE TERRARUM PROGRESSUM SYSTEMATUM ELECTRONICAE ENERGIAE INVESTIGATIONUM PROMOVIT, IMPRIMIS AUTEM EFFECIT, UT COMMUTATORES POTENTIAE TRANSISTORII MULTA PLANITIE AUCTI MELIORES AC MELIORES STRUERENTUR

DOCTORIS HONORIS CAUSA
SCIENTIARUM TECHNICARUM

NOMEN AC DIGNITATEM, IURA AC PRIVILEGIA CONTULIMUS IN EIUSQUE REI FIDEM HOC DIPLOMA SIGILLO POLYTECHNICAE LUBLINENSIS SANCIENDUM CURAVIMUS

SBYGNEUS PATER

H. T. RECTOR MAGNIFICUS

ADALBERTUS JARZYNA

PROMOTOR

PAULUS WĘGIEREK

H. T. DECANUS

LUBLINI, DIE XII MENSIS MAII A. D. MMXXII

Prof. dr hab. inż. Wojciech Jarzyna
Kierownik Katedry Napędów i Maszyn Elektrycznych

LAUDACJA

z okazji nadania profesorowi Gopakumarowi Kumarukuttan Nair godności Doktora Honoris Causa Politechniki Lubelskiej

Magnificencjo Rektorze,
Wysoki Senacie,
Czcigodni Doktorzy Honoris Causa,
Profesorowie Honorowi Politechniki Lubelskiej,
Wielce Dostojni Goście

Z woli Senatu Politechniki Lubelskiej, na wniosek Rady Dyscypliny Naukowej Automatyki, Elektroniki i Elektrotechniki oraz wobec jednoznacznie pozytywnych recenzji przyjętych przez Wysokie Senaty znakomitych europejskich uczelni takich jak University of Sevilla, Bergische University of Wuppertal i Politechniki Warszawskiej, mam zaszczyt wygłosić laudację komplementującą osiągnięcia naukowe i zasługi w kształceniu kadry naukowej profesora Gopakumara Kumarukuttan Nair z Indian Institute of Science.

Profesor Gopakumar K. jest światowej sławy naukowcem specjalizującym się w obszarze energoelektroniki. Jego pionierskie rozwiązania przekształtników energoelektronicznych i napędów elektrycznych są wysoko cenione na całym świecie. W międzynarodowym środowisku naukowym rozpoznawany jest jako jeden z najbardziej innowacyjnych badaczy w zakresie topologii wielopoziomowych energoelektronicznych układów przekształtnikowych oraz zaawansowanych metod modulacji i zastosowań układów energoelektronicznych w wysokiej klasy systemach napędowych.

Główne zainteresowania badawcze prof. Gopakumara obejmują m.in. sterowanie napędami o regulowanej prędkości za pomocą falowników napięcia do 17 i 49 poziomów. Zajmując się tą tematyką prof. Gopakumar opracował wiele nowych topologii falowników do zastosowań w napędach dużej mocy. Zadaniem tych wielopoziomowych rozwiązań jest generowanie sinusoidalnego przebiegu napięcia pozbawionego harmonicznych niskiego rzędu. Rozwijając te układy Profesor, wraz ze swoim zespołem badawczym, projektuje i uruchamia przekształtniki, dla których tworzy zaawansowane wielostronne wielopoziomowe metody modulacji wektorów przestrzennych napięcia oparte o struktury wieloboków foremnych. Opracowane innowacyjne rozwiązania wyznaczają kierunki rozwoju układów energoelektronicznych do zastosowań w napędach elektrycznych i w sprzęgach energoelektronicznych dla energetyki rozproszonej.

Wybitne osiągnięcia naukowe, stworzenie silnego zespołu badawczego oraz wypromowanie szeregu młodych i zdolnych naukowców składają się na szkołę naukową profesora Gopakumara. Wypromował On 29 doktorów, a kolejnymi sześcioma opiekuje się obecnie. Jego wychowankowie pracują w czołowych uczelniach i firmach na świecie,

a osiągane przez nich sukcesy w USA, Kanadzie i Europie najlepiej świadczą o randze szkoły naukowej jaką otrzymali od swojego mistrza i mentora.

Profesor Gopakumar ma znakomity dorobek publikacyjny, na który składa się blisko 300 tytułów w czasopismach i materiałach konferencyjnych. Wszystkie są publikowane przez prestiżowe wydawnictwa takie jak IEEE, IET, IEE i EPE, a liczba ich cytowań jest imponująca. Świadczą o tym indeksy Hirscha 32, 42 i 45, odpowiednio w WoS, Scopus i Google Scholar.

W uznaniu osiągnięć naukowych Profesora Gopakumara w stowarzyszeniach branżowych IEEE, INAE i IETE przyznano mu status członkowski Fellow Member. Jest On także współredaktorem czasopisma IEEE Industrial Electronics. Posiada tytuł distinguished lecturer IEEE Industrial Electronics Society. W 2019 roku został wyróżniony prestiżową nagrodą IEEE Eugene Mittleman Outstanding Research Achievement Award, która jest najwyższą nagrodą techniczną przyznawaną przez stowarzyszenie IEEE – IES. Profesor Gopakumar otrzymał wiele cennych nagród, w tym nagrodę indyjskiego stowarzyszenia IETE im. prof. B.K. Bose za wkład w obszar energoelektroniki i napędów dużej mocy, nagrodę macierzystej uczelni Indian Institute of Science - Alumni za doskonałość w badaniach w inżynierii w 2016 r. oraz tytuł ABB Chair Professor (2016 – 2018).

Z profesorem Gopakumarem poznaliśmy się na międzynarodowej konferencji European Power Electronics w Warszawie w 2017r. Szybko nawiązaliśmy intensywną, owocną współpracę badawczą w obszarze sterowania układów energoelektronicznych jak i w kształceniu doktorantów. Dużą rolę w umacnianiu naszej współpracy odegrało Stowarzyszenie IEEE oraz wspólne inicjatywy realizowane z Zakładem Elektroniki Przemysłowej Politechniki Warszawskiej reprezentowanym przez profesorów Mariana P. Kaźmierkowskiego, Mariusza Malinowskiego i Marka Jasińskiego.

Wyrazem bezpośredniej współpracy z profesorem Gopakumarem są jego wykłady prowadzone na Politechnice Lubelskiej. Wypełnione są one pełnymi pasji i wielkiego zaangażowania dysputami naukowymi z pracownikami i doktorantami. Efektem wspólnych badań są publikacje w czasopismach o najwyższej, w inżynierii elektrycznej, randze światowej. W 2020 r. Profesor Gopakumar był recenzentem rozprawy doktorskiej, za którą nasza doktorantka. otrzymała nagrodę Prezesa Rady Ministrów RP. W środowisku międzynarodowym, w tym na posiedzeniach plenarnych IEEE, jest aktywnym patronem Politechniki Lubelskiej komplementując wysoki poziom badań i dużą dynamikę młodego zespołu naukowego Naszej Uczelni. Jest urzeczony polską kulturą i przyrodą. Zdarza się, że podczas podróży poza miasto prosi o zatrzymanie się by podziwiać żółte łany majowego rzepaku, czy soczystą zieleń lasu. Zna polską historię, zwłaszcza okres związany z II Wojną Światową. Zawsze wzrusza się odwiedzając miejsca związane z martyrologią jak Majdanek, Oświęcim, Bełżec i inne.

Dzisiejsza uroczystość nadania godności Doktora Honoris Causa profesorowi Gopakumarowi Kumarukuttan Nair to wielkie święto dla naszej społeczności akademickiej oraz międzynarodowego środowiska naukowego power electronics i stowarzyszenia IEEE. Panie Profesorze cieszymy się, że razem możemy świętować to doniosłe wydarzenie.

Lublin, 12.05.2022 r.

Prof. Wojciech Jarzyna
Head of the Electrical Drive and Machine Department

LAUDATION

on the occasion of awarding professor Gopakumar Kumarukuttan Nair with the title of Doctor Honoris Causa of the Lublin University of Technology

Your Magnificence,
High Senate,
Honourable Honorary Doctors,
Honorary Professors of the Lublin University of Technology,
Esteemed Guests

By the will of the Senate of the Lublin University of Technology, at the request of the Scientific Discipline Council of Automation, Electronics and Electrical Engineering, and in view of the unequivocally positive reviews received by the High Senates of outstanding European universities, such as the University of Sevilla, Bergische University of Wuppertal and the Warsaw University of Technology, I have the honour of delivering a laudation complementing the scientific achievements and contribution to the training of academic staff of Professor Gopakumar Kumarukuttan Nair from the Indian Institute of Science.

Professor Gopakumar K. is a world-renowned scientist specialising in the field of power electronics. His pioneering solutions of power electronic converters and electric drives are highly appreciated all over the world. In the international scientific community, he is recognised as one of the most innovative researchers in the field of multi-level power electronic converter system topologies and advanced modulation methods and applications of power electronic systems in high-class drive systems.

The main research interests of prof. Gopakumar include control of variable speed drives with multilevel voltage inverters up to 17 and 49 levels. Dealing with this subject, prof. Gopakumar has developed many new inverter topologies for high power drive applications. The task of these multilevel solutions is to generate a sinusoidal voltage waveform devoid of low-order harmonics. By developing these systems, the Professor, together with his research team, designs and launches converters for which he creates advanced multisided multilevel voltage space vector modulation methods based on regular polygon structures. The developed innovative solutions set the directions for the improvement of power electronic systems for applications in electric drives and in grid-tied smart power electronic converters interacting with distributed energy sources.

Outstanding scientific achievements, the creation of a strong research team and the promotion of a number of young and talented scientists make up Professor Gopakumar's science school. He promoted 29 doctors, and is currently looking after another six. His PhD alumni work in leading universities and companies in the world and their successes in the USA, Canada and Europe are the best proof of the rank of the scientific schooling they received from their master and mentor.

Professor Gopakumar has an excellent publication record, which includes nearly 300 titles in journals and conference proceedings. They are all published by prestigious publishing houses such as IEEE, IET, IEE and EPE, and the number of their citations is impressive. This is evidenced by the Hirsch indexes 32, 42 and 45, respectively in WoS, Scopus and Google Scholar.

In recognition of Professor Gopakumar's scientific achievements in the engineering associations IEEE, INAE and IETE, he was granted the Fellow Member status. He is also a co-editor of the IEEE Industrial Electronics magazine. He holds the title of distinguished lecturer of the IEEE Industrial Electronics Society. In 2019, he was awarded the prestigious IEEE Eugene Mittleman Outstanding Research Achievement Award, which is the highest technical award granted by the IEEE-IES Society. Professor Gopakumar has received many valuable awards, including the Indian Prof. B. K. Bose IETE society award for his contribution to the area of power electronics and high power drives, the award of his home Indian Institute of Science university – IISc Alumni for Excellence in Research in Engineering in 2016 and the title of ABB Chair professor (2016-2018).

We met Professor Gopakumar at the International European Power Electronics conference in Warsaw in 2017. We quickly established intensive, fruitful research cooperation in the field of power electronic systems control as well as in the education of doctoral students. The IEEE association and joint initiatives carried out with the Division of Industrial Electronics of the Warsaw University of Technology, represented by professors Marian P. Kaźmierkowski, Mariusz Malinowski and Marek Jasiński, played a significant role in strengthening our cooperation.

An expression of direct cooperation with professor Gopakumar are his lectures at the Lublin University of Technology. They are filled with passionate and commited scientific disputes with academic staff and doctoral students. The result of joint research are publications in journals of the highest global rank in electrical engineering. In 2020, Professor was a reviewer of the doctoral dissertation, for which our doctoral alumna received the Prime Minister's of the Republic of Poland award. In the international community, including at IEEE plenary meetings, he is an active patron of the Lublin University of Technology, complimenting the high level of research and great dynamics of the young research team of our University. He is captivated by Polish culture and nature. It is not unusual of him, when travelling outside the city here, to ask you to stop to admire the yellow fields of May rape or the lush green of the forest. He knows Polish history, especially the period related to World War II. He is always moved when visiting places related to martyrdom, such as Majdanek, Oświęcim, Bełżec and others.

Today's ceremony of granting the title of Doctor Honoris Causa to Professor Gopakumar Kumarukuttan Nair is a great celebration for our academic community and the international power electronics research community as well as the IEEE association. Dear Professor, we are very glad that we can celebrate this important event together.

Lublin, 12.05.2022 r.

Uchwała nr 456/XLIX/2020
Senatu Politechniki Warszawskiej
z dnia 22 stycznia 2020 r.

w sprawie poparcia inicjatywy nadania tytułu doktora honoris causa prof. Gopakumar Kumarukuttan Nair przez Politechnikę Lubelską

Na podstawie § 42 ust. 2 pkt 3 Statutu PW oraz w związku z wystąpieniem Senatu Politechniki Lubelskiej, uchwala się, co następuje:

§ 1

Po zapoznaniu się z dorobkiem naukowym prof. Gopakumar Kumarukuttan Nair, Senat Politechniki Warszawskiej postanawia poprzeć inicjatywę nadania mu tytułu doktora honoris causa przez Politechnikę Lubelską.

§ 2

Uchwała wchodzi w życie z dniem podjęcia.

Sekretarz Senatu
mgr Beata Dobrzeniecka

Rektor
prof. dr hab. inż. Jan Szmidt

Kierownik Biura Rektora
dr Agnieszka Kamińska

Prof. zw. dr hab. inż. Marian P. Kaźmierkowski
Członek rzeczywisty PAN, IEEE Life Fellow
Politechnika Warszawska
Wydział Elektryczny

Warszawa, 18.01.2020 r.

O P I N I A

Dla

Senatu Politechniki Warszawskiej w sprawie przyznania Prof. Gopakumar Kumarukuttan Nair zasłużonego tytułu DOKTORA HONORIS CAUSA Politechniki Lubelskiej

Prof. K. Gopakumar uzyskał w Indian Institute of Science, Bangalore w dyscyplinie Elektrotechnika kolejno tytuły licencjata (BSc) w 1980 roku następnie mgr inż. (MSc) w 1984 oraz dr inż. (PhD) w 1994 r. Tytuł pracy magisterskiej „Szeregowy falownik prądu zasilający silnik indukcyjny z dzielonymi uzwojeniami" a tytuł pracy doktorskiej był „Badanie napędu z silnikiem indukcyjnym z dzielonymi uzwojeniami zasilanym z falownika napięcia".

Aktualnie jest profesorem na Wydziale Inżynierii Systemów Elektronicznych (dawniej CEDT - Centrum Projektowania i Technologii Elektronicznej) w Indian Institute of Science (IISc), Bangalore, Indie.

Po uzyskaniu magisterium w latach 1984-1987 pracował w Space Research Organization, Satellite Center, Bangalore przy projektowaniu i budowie satelitarnych systemów zasilania pokładowego SROSS-1 (Stretched Rohini Satellite Series-1).

Od 1987 r. został zatrudniony w CEDT - Centrum Projektowania i Technologii Elektronicznej, Indian Institute of Science w Bangalore, jako pracownik naukowy, a następnie po uzyskaniu doktoratu kolejno, jako adiunkt (1997), profesor nadzwyczajny (2003) oraz profesor (2007).

Mam przyjemność znać prof. Gopakumara od 16 lat, jako jednego z wielu kolegów w społeczności energoelektroniki oraz jako partnera w badaniach. Mój pierwszy pośredni kontakt z działalnością prof. Gopakumara sięga 2004 roku, kiedy wówczas jako redaktor naczelny czasopisma IEEE Transactions on Industrial Electronics (2004-2006) zaprosiłem go do składu redakcyjnego jako Associate Editor, i przez te ostatnie szesnaście lat Jego działalność zarówno w Redakcji Transactions (gdzie awansował i w latach 2016-2018 był Co-editor in chief) jak i jako wolontariusz w ramach Industrial Electronics Society (IES) były wzorowe. Od tego czasu regularnie odwiedza Polskę, wygłaszając wykłady dla studentów studiów magisterskich i doktoranckich w Politechnice Warszawskiej, Politechnice Wrocławskiej i nade wszystko w Politechnice Lubelskiej.

Jego działalność jest przykładem prawdziwego lidera pracującego w ważnym obszarze analizy i sterowania układów energoelektronicznych. Dziś jest jednym z wiodących ekspertów, uznanym na arenie międzynarodowej w dziedzinie wielopoziomowych topologii falowników, sterowania napędami o regulowanej prędkości, a także jednym z najbardziej cytowanych badaczy w tej dyscyplinie. W swojej macierzystej uczelni Indian Institute of Science w Bangalore w 1998 roku zorganizował grupę badawczą, która zyskała powszechne uznanie. Jego główny wkład dotyczy trzech powiązanych, ale bardzo wyraźnych obszarów w szerokiej tematyce przekształtników i napędów średniej i wielkiej mocy: (1) wielofazowe napędy silników indukcyjnych, (2) wielopoziomowe topologie falowników dla napędów silników indukcyjnych (ang. Induction Motor - IM) i (3) metody modulacji wektorowej do sterowania napędami IM zasilanymi z falowników wielopoziomowych. Jest pionierem w zakresie prac nad napędami wielofazowymi (asymetryczne sześciofazowe silniki indukcyjne z wykorzystaniem falowników napięcia (ang. Voltage Source Inverter - VSI)). Opublikował również pierwsze wyniki eksperymentalne przy niezależnym sterowaniu systemem dwóch silników połączonych szeregowo zasilanych z układu falownika z pojedynczym źródłem napięcia. Jego pionierskie prace badawcze w dziedzinie falowników wielopoziomowych zaowocowały licznymi nowymi topologiami oraz wektorowymi metodami modulacji wektorowej napięcia do 17 i 49 poziomów. Jest także jednym z pionierów w wielopoziomowej topologii napędów IM z uzwojeniem otwartym. Takie topologie mają prostą strukturę szyny zasilającej, ze zwiększoną liczbą redundancji stanów łączeń, w porównaniu z dowolnym konwencjonalnym systemem wielopoziomowym dla napędów IM z izolowanym punktem neutralnym. Opracował także całkowicie oryginalne i

nowatorskie wielopoziomowe topologie falowników oparte na generowaniu 12-stronnych wielopoziomowych wektorów napięcia, co skutkuje redukcją niskich harmonicznych do 29 i 31 rzędu, ze zwiększonym zakresem modulacji. Są one bardzo przydatne w napędach o zmiennej prędkości z prawie sinusoidalnymi napięciami wyjściowymi w całym zakresie modulacji i mogą być uważane za falownik bez filtra z prawie sinusoidalnymi napięciami wyjściowymi. Trzeci obszar, w którym prof. Gopakumar wniósł znaczący wkład, związany jest ze sterowaniem falowników wielopoziomowych z wykorzystaniem wektorowych metod modulacji szerokości impulsów SVM.

Tak intensywne wysiłki badawcze znajdują odzwierciedlenie w jego bogatym dorobku naukowym:

- **109 artykułów w czasopismach** najwyższej rangi jak IEEE Transactions, IEE Proceedings (później IET), EPE Journal, etc.
- **85 referatów prezentowanych** na konferencjach międzynarodowych i publikowanych w materiałach konferencyjnych.

W bazie Web of Science Core Collection posiada ponad 6000 cytowań oraz indeks Hirscha h = 32.

Prof. Gopakumar, jako wspaniały motywator i promotor wypromował 27 doktorów, a aktualnie pod Jego opieką pracuje 6 doktorantów. Ponadto był kierownikiem 10 zakończonych projektów badawczych oraz 13 projektów wykonanych na zlecenie przemysłu, w większości dla koncernów międzynarodowych mających oddziały w Indiach (Infosys Technologies Ltd., JVS Electronic Ltd., DASAG Energy Engineering Ltd. Seuzach, Switzerland, General Motors, Honeywell India).

Dlatego uznając w pełni niezwykłą pozycję i zasługi Prof. **Gopakumar Kumarukuttan Nair, jako** wybitnego uczonego i nauczyciela akademickiego, a nade wszystko Jego intensywną wzorową współpracę oraz wkład w rozwój Wydziału Elektrotechniki i Informatyki Politechniki Lubelskiej, której jest On niestrudzonym ambasadorem na arenie międzynarodowej, rekomenduję **Senatowi Politechniki Warszawskiej wyrażenie pełnego poparcia dla przyznania Mu tytułu Doktora Honoris Causa Politechniki Lubelskiej.**

Prof. zw. dr hab. inż. Marian P. Kaźmierkowski

BERGISCHE
UNIVERSITÄT
WUPPERTAL

DER REKTOR
Prof. Dr. Dr. h.c. Lambert T. Koch

Bergische Universität Wuppertal, Prof. Dr. Dr. h.c. Lambert T. Koch,
Gaußstraße 20, 42119 Wuppertal

Prof. dr hab. inz. Piotr Kacejko
Rector
Lublin University of Technology
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Datum 12.02.2020

Estimated Colleague, dear Rector Kacejko,

Thank you very much for your trust in Prof. em. Joachim Holtz to act as a reviewer in the context of the planned awarding of a honorary doctorate to Prof. Gopakumar Kumarukuttan.

Enclosed to this letter, I have the pleasure to forward you the detailed expert opinion by Prof. em. Joachim Holtz, who will also be glad to answer any question that may arise in this regard.

With kind regards from Wuppertal,

Lambert T. Koch

BERGISCHE UNIVERSITÄT WUPPERTAL

Fachbereich E
ELEKTROTECHNIK
INFORMATIONSTECHNIK
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Prof. Dr. J. Holtz Am Forsthof 16 42119 Wuppertal

To
Prof. Piotr Kacejko
Rector
Lublin University of Technology
Poland

Wuppertal, 2. February 2020

Ref: Conferring the title of Doctor Honoris Causa to Prof. Gopakumar K. Nair

Dear Prof. Kacejko,

It gives me great pleasure being a reference for conferring the title of Doctor Honoris Causa to Prof. Gopakumar Kumarukuttan Nair.

I came to know Prof. Gopakumar during my frequent visits to India, having been a Professor at the Indian Institute of Technology in Madras from 1969 to 1972. During the following years I have kept close contacts with my colleagues of many Indian Universities, and I also visited the Indian Institute of Science (IISc.) in Bangalore many times as a Distinguished Lecturer of the IEEE Industrial Electronics Society. I also met Prof. Gopakumar frequently on IEEE conferences all over the world. Given our common research interests, we used to discus current research problems and exchange the results of our respective research activities. It so happened that we both investigated on an inverter topology that comprises two series connected three-level converters fed from a common dc link circuit. Our discussions related frequently to the respective pulsewidth modulation methods that we used were different with respect to optimal pulse patterns that satisfy different objective functions at the same time, namely minimum harmonic distortion and minimum, and mode voltage.

Prof. Gopakumar is one of the leading international experts on multilevel inverter topologies and their control for variable speed drive applications. He is a highly cited scientist in this field. His main contributions relate to three distinct areas of a broad topic: Power Electronic Converters and Drive Control. These are classified as

1. **Multilevel inverter topologies for induction motor drives**
   Among the inventions on this topic are:
   - A 17-level inverter topology with low component count for open-end motor windings,
   - A modulation scheme to generate a 12-level polygonal-sided switching state vector pattern,
   - A topology comprised of a number of low voltage stacked and cascaded inverter cells to generate a 12-sided switching state pattern,
   - A general modulation strategy to generate n-level switched waveforms
   - A 17-level inverter topology formed by cascading flying capacitor and floating capacitor H-bridges
   - A topology formed by cascading three-level and two-level inverters

2. **Multilevel inverter topologies with a single dc-link**
   Among the inventions on this topic are:
   - extended linear modulation operation of a common mode voltage eliminated cascaded multilevel inverter with a single dc supply
   - A three-level dodecagonal switching state vector-based harmonic suppression
     scheme for open and winding induction motor drives with single dc supply
   - Fifth and seventh order harmonic elimination with multilevel switching state vector structure for induction motor drive using a single dc source for the full speed range
   - Multilevel switching state vector structure generation for open-and winding induction motor using a single dc source
   - Low order harmonic suppression for open-and winding induction motor with dodecagonal switching state vector using a single dc-link supply reduced common mode voltage operation of a new seven-level hybrid inverter topology with a single dc voltage source

3. **Pulsewidth modulation techniques**
   Among the inventions on this topic are:
   - A medium voltage inverter fed induction motor drives using multilevel 12-sided switching state vectors with nearly constant switching

frequency current hysteresis controller
- Hysteresis current controller for the general *n*-level inverter fed drive with online current error boundary computation and nearly constant switching frequency
- A predictive capacitor voltage control of a hybrid cascaded multilevel inverter with a single DC link and reduced common mode voltage operation
- Nearly constant switching frequency hysteresis current controller with fast online computation of boundary for a 2-level voltage source inverter fed induction motor

4. Industrial consultancy

Prof. Gopakumar has completed a total of 12 industrial consultancy projects which resulted from his inventions.
- NGEF Ltd. Duration October 1993 to June 1995
- Infosys technologies Ltd. Duration June I 1994 to August 1959
- Bharat Heavy Electricals, Duration August 1993 to May 1995
- JVS Electronic Ltd. Duration October 1994 to March 1996
- IPA Private Ltd.
- Foresight Power Systems Private Ltd.
- Wheeler Vehicles
- General Motors, USA
- Honeywell India

5. Projects funded by The Department of Electronics, Government of India
- A regenerative electronic load fed by a three-phase rectifier which then feeds the power into the three-phase mains
- Studies on multi-level inverter fed induction motor drives schemes with common mode voltage elimination
- A five-level inverter scheme with common mode voltage suppression and dc link capacitor balancing for induction motor drives for high power applications
- A multi-level 12-sided polygonal switching state vector structure for high power induction motor drives applications

6. Prof. Gopakumar's engagement for Lublin University of Technology

Professor Gopakumar K.'s collaboration with the Lublin University of Technology (LUT) goes back to 2017. It developed in research and didactic areas. The first classes he conducted in September 2017. In the following years, he was invited here as a visiting professor. During these visits, he held

numerous seminars and lectures. Some of them are documented in the Internet, e.g. on the IEEE Poland Section web pages.

Especially strong connections were established with a group of young scientists working in the power electronics laboratory at the Department of Electrical Drives and Machines, headed by Professor W. Jarzyna. Professor Gopakumar K. spent a lot of time there, explaining the methodology of research work and discussing a number of topics of interest to young scientists.

He took part in a Ph.D. defense. By the research council of the Faculty of Electrical Engineering and Computer Science of the LUT, he was designated as a reviewer of a Ph.D. dissertation.

Indicators for collaboration evaluation include signed and implemented contracts, joint projects, and publications. In this case, these factors are very high and are confirmed by agreements between the IIS and the LUT, a bilateral Erasmus+ agreement and high-level research papers he has published. Further perspectives also look promising. A direct exchange of achievements is developing, and doctoral students from the LUT have the possibility to develop scientific articles under the guidance of Professor Gopakumar.

To summarize, Professor Gopakumar has excelled in the extreme broad area of power electronics and motor control. He has a profound knowledge in an expanded field, not only as an academic but also with a deep understanding of what is needed by industries.

Bearing in mind the facts contained in this opinion, I am convinced that the entire research achievements of Prof. Gopakumar K., as well as his position and authority in the international scientific community, fully justify bestowing upon him the title of Doctor Honoris Causa.

With best regards,

Prof. em. Dr.-Ing. J. Holtz

UNIVERSIDAD D SEVILLA
EL RECTOR

Seville, February, 17th, 2020

Prof. Piotr Kacejko
Rector
Lublin University of Technology

Dear Rector,

Please, find attached a positive opinion on behalf of the scientific community of the University of Sevilla by Professor Leopoldo Garcia Franquelo about the achievements and research activities of prof. Gopakumar Kumarukuttan Nair from the Indian Institute of Science, in relation to the initiation of the procedure of granting prof. Gopakumar K. the title of Doctor Honoris Causa of the Lublin University of Technology.

Yours sincerely,

Miguel Ángel Castro Arroyo
Rector
University of Seville

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OPINION on granting Professor Gopakumar Kumarukuttan Nair the title and dignity of Doctor Honoris Causa of the Lublin University of Technology

I met personally Prof. Gopakumar more than 20 years ago while I was attending international conferences in the industrial electronics area.

Prof. Gopakumar is one of the most important international researchers in the power electronics area in the last decades. He is internationally recognized as one of the most innovative researchers in topics such as high-power converter topologies, modulation and control methods for motor drives applications. His contributions to the development of efficient, robust and economically affordable power converters are outstanding, looking for industrial solutions to cover all the requirements of actual applications in diverse fields, like renewable energies sources connection to the power grid.

Prof. Gopakumar owns a deep experience in the power electronics area initially being employed in the Indian Space Research Organisation developing satellite on board power supply systems (related to Stretched Rohini Satellite Series). Since 1987, Prof. Gopakumar has been working in the Indian Institute of Science of Science, Bangalore, India. He has been working with different positions being finally promoted to full professor in 2007. In his more than 35 years of working experience, he has been incredibly active in many academic, industrial, research and innovation activities being one of the most active persons in the area.

As a researcher, Prof. Gopakumar is one of the most well-recognized researchers developing new power converter topologies for high-power applications. Specifically, many of his contributions are related to introduce different multilevel power converters, which are one of the most successful solutions for high-power systems of the last 20 years. His contributions have contributed in a decisive way to the development of this kind of solutions to become an actual industrial solution for important applications such as fans, pumps, integration of renewable energy sources, flexible ac transmission systems, high-voltage dc transmission systems and high-power motor drives. His original innovations in this area have contributed to develop new topologies based on modular solution leading to achieve enhanced output waveforms quality also adding features such as reduced cost, high efficiency and fault tolerant capability. Many of these solutions are based on hybrid converters taking the advantages of mature power modules being connected wisely in order to obtain the best performance. Many of Prof. Gopakumar's ideas are the base of new

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solutions to be applied to specific applications where the requirements are very strict in terms of power quality, controllability and reduced cost.

Variable-speed motor drives is other research topic where Prof. Gopakumar has been focused during his research career. Specifically, many of his works are related to the development of open-end windings induction motor drives which fit with his contributions related to multilevel converters. His contributions in this field have opened new research lines for the industry looking for efficient motor drive solutions with advantages such as (1) power equalization from both sides of each winding what leads to a reduction in the nominal power of the power modules, (2) enhanced controllability of the phase stator currents, (3) reduction of common-mode voltages (what is the one of the main causes of the machine damage) and (4) fault tolerance capability. Prof. Gopakumar is one of the leaders of this attractive concept that is considered as a proper solution for many applications in a wide nominal power range, from medium to high-power.

On the other hand, Prof. Gopakumar is one of the most recognized researchers developing new modulation techniques of advanced power converter topologies. His advances related to space-vector modulation methods for complex power converters are very well-known. His contributions related to this area present outstanding performance, high simplicity and reduced computational cost. His modulation strategies not only are focused on the generation of the output waveforms with optimal quality but also include internal control methods to deal with critical targets as the control of floating dc voltages in the power modules. This was the barrier to consider many power converters as actual solutions for industrial applications and Prof. Gopakumar's contributions have overcome these challenges. This opened the possibility to use modular converters with enhanced controllability in a wide modulation index range and with optimal waveforms quality.

Prof. Gopakumar always introduces the new solutions in very educational way making his contributions as key works for all the industry and the academia. In fact, Prof. Gopakumar can be considered as one of the most influential researchers all over the world in the power electronics area in the last decade. He has received more than 10000 citations being the inspiration of many young and senior researchers, motivating new original ideas and looking for novel solutions for actual industrial applications.

One important issue to highlight is that Prof. Gopakumar is one researcher with outstanding emphasis on spreading their knowledge, especially to novel researchers. In fact, his experience as manager of his research group has given him the opportunity to teach new researchers that have also become with the years internationally recognized researchers. We

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want to highlight his impressive work as teacher and leader of the new generations, what is the main objective of a university. His work as professor in his university and his speeches in multiple tutorials and seminars are a valuable proof of this issue. Another important key work of Prof. Gopakumar to collaborate with the research dissemination is related to his activities in the Institute of Electrical and Electronics Engineers (IEEE) where he is deeply involved, mainly with the Industrial Electronics Society (IES). The IEEE is the largest association of electrical and electronics engineers formed by more than 400000 members from 170 countries all around the world, publishing the most prestigious journals and organizing the best-reputed conferences in the area. Prof. Gopakumar was serving as Associate Editor and Co-Editor in Chief of the journal IEEE Transactions on Industrial Electronics, one of the journals of highest impact factor of the area. In addition, he has collaborated with the organization of multiple important international IEEE conferences, special sessions, etcetera.

As a result of his contributions, Prof. Gopakumar has received many recognitions during his professional career. As a token of his well recognized trajectory as a researcher, it can be mentioned that he was elevated to IEEE Fellow in 2012 "For contributions to design and control of multilevel converters". IEEE Fellow is the maximum technical distinction in IEEE and only one per 1000 of the membership are selected as IEEE Fellows. Also in 2019 he was the recipient of the IES Dr.-Ing. Eugene Mittelmann Achievement Award "For contributions to the development of new topologies and the control of multilevel inverters for drives". This award is the most important distinction that the IEEE-IES confers.

Prof. Gopakumar is recognized worldwide and he has been invited to many of the most important research centers in the world. It is important to mention that he has been appointed as an IES Distinguished Lecturer. For this reason, he is frequently invited by many universities worldwide. His lectures are inspiring engineers, motivating new ideas and pushing creativity.

As I mentioned before, the relation between Universidad de Sevilla and Prof. Gopakumar started almost 20 years ago, where I met him in international conferences organized by the Industrial Electronics Society. Since then, Prof. Gopakumar is working very closely with the power electronics group of our university where I belong. This very successful collaboration has led many research publications with symbiotic beneficial results for both institutions from India and Spain. Our cooperation has been very close and productive and includes 12 papers in high impact journals and 11 papers in international conferences. In addition, Universidad de Sevilla got the chance of enjoying Prof. Gopakumar lectures in 2014, when

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he was visiting our university collaborating in an Erasmus+ European Project called Heritage.

The collaboration with Prof. Gopakumar has been very important to our university helping us to improve our research, opening new research lines and keeping close contact with many other research institutes worldwide where Prof. Gopakumar already had collaborations. His generosity has permitted us to grow and now the power electronics group of our university can be considered as one of the most well-known research groups in the world.

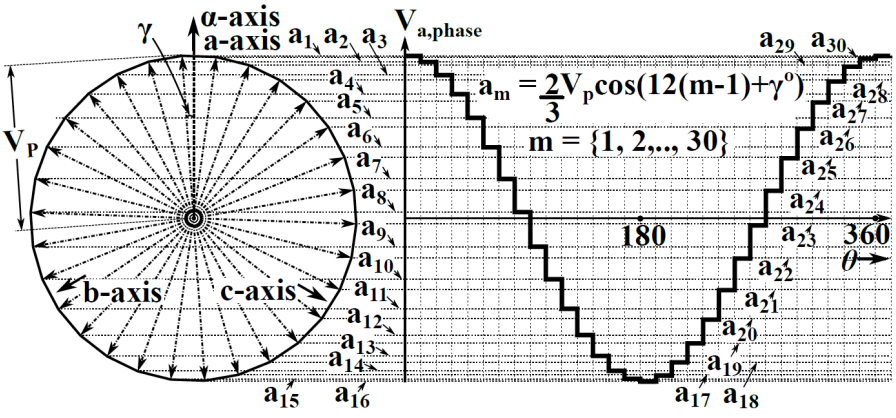
For all these reasons, I consider him as the best candidate to receive the Doctor Honoris Cause distinction from Lublin University of Technology.

In Sevilla, February 17, 2020

Signed Leopoldo Garcia Franquelo
Professor,
Departamento de Ingenieria Electronica,
Universidad de Sevilla
Escuela Superior de Ingenieros
Camino de los Descubrimientos s/n
41092 Sevilla, Spain

DC to AC Power Converter Topologies for Industrial drives and Grid tied applications

Prof. Gopakumar Kumarukuttan Nair



DC to AC Power Converter Topologies for Industrial drives and Grid tied applications

Prof. K. Gopakumar, DESE, Indian Institute of Science, Bangalore INDIA

1. Voltage source converters

Power electronic converters facilitate efficient control and conversion of electrical power, a requirement in almost all modern equipments and systems. Power loss is an unavoidable consequence of the energy conversion process. However, power electronic energy conversion provides the means to minimize these losses and achieve higher efficiency. This aspect of power electronic converters is very significant in the present world scenario characterized by the ever increasing demand for power on one side and the depletion in the available energy resources on the other side. The need of the hour is to minimize the power loss as the energy saved is equivalent to additional energy generated with the same resources. In the field of high power applications a small improvement in the efficiency is significant as it will result in substantial energy savings. Hence it is all the more important to improve the efficiency of energy conversion in high power applications. Advanced and sophisticated control is another requirement in many modern applications. The power electronic converters can be broadly classified into four categories. They are: (i) DC to DC converters (ii) AC to DC converters (iii) DC to AC converters and (iv) AC to AC converters [1]. Major high power applications of these converters include high and medium- voltage drives, flexible AC transmission systems (FACTS), active power filters, reactive power compensation systems, renewable energy sources etc. [2]-[3]. The DC to AC converters are widely used in control of drives, which constitute around 60-65% of the total load on the electrical energy distribution systems [4]. There are basically two types of DC to AC converters namely the voltage source inverters (VSI) and the current source inverters (CSI). Though the current source inverters (CSI) have significant presence in certain high power applications, the voltage source inverters (VSI) are now dominating the field of DC to AC conversion, due to their inherent advantages like relatively simpler circuit configurations and emergence of semiconductor devices whose performance and characteristics meet the requirements of the VSI topology.

2. Two-level voltage source converters

The traditional DC to AC voltage source converters are known as two level inverters as they switch between two voltage levels. The power can be made to flow in both the directions and hence it can work as rectifier as well as inverter. Hence a better name for the circuit is voltage source converter.

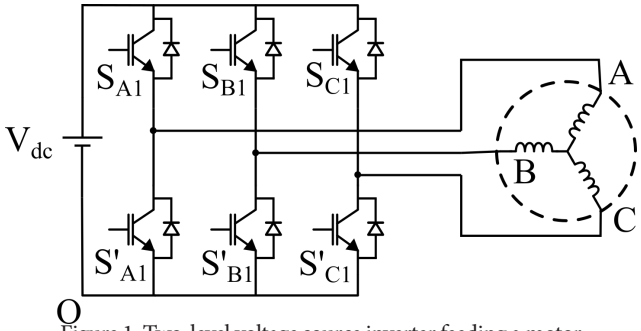


Figure 1. Two-level voltage source inverter feeding a motor

In two level inverter the A-phase can be connected to the postive terminal of the DC voltage by switching on the switch S_A '(S_{A1} ' is off) and to the negative terminal by switching off S_A ' (S_{A1} ' is on). The respective phase-A pole voltage is shown in Fig. 2a and its harmonic content is shown in Fig.2b. To get the fundamental sinusoidal component, it is easy to say that we can remove all the harmonics by putting a filter. But in practise a filter to remove all the harmonics in Fig.2b is impractical because we need very bulky filters and cost of it alone will be much higher than the inverter and its control.

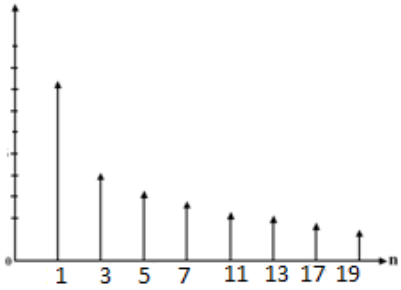


Figure 2a. Output pole voltage waveform

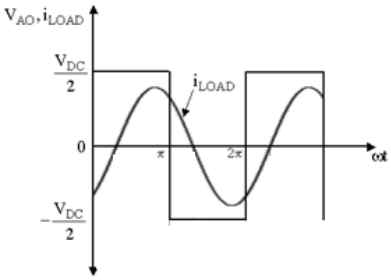


Figure 2b.Harmonic spectrum

But the effect of the harmonic voltages can be controlled in the output current waveform, by using the pulse width modulation(PWM) technique known as the sine-triangle PWM. Here a sine wave called the modulating wave(which is proportional in amplitude and in phase with the output fundamental wave to be generated from the inverter)is compared with a fixed amplitude high frequency triangle waveform to generate the gating signals. Same triangle wave is compared with sine waves representing the out fundamental wave of the three phase outputs, to generate the gating signals for the inverter. When the sine wave is greater than the triangle wave (carrier wave) in each phase, the top switch is ON and the bottom switch is OFF. When the amplitude of sine wave form is less than the triangle then the top switch is OFF and the bottom switch is ON. This way the original square wave of Fig.2a is chopped with a high frequency and the typical output pole voltage of a phase is shown in Fig.3a.

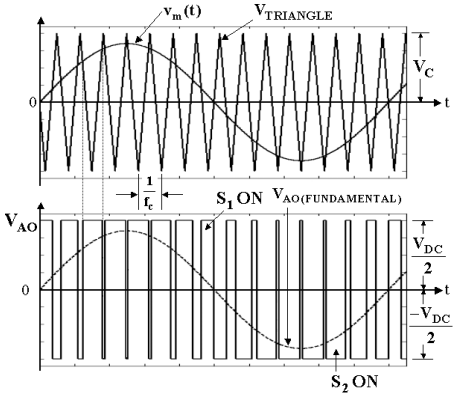


Fig 3a. Pole voltage waveform
(Sine-triangle Comparison)

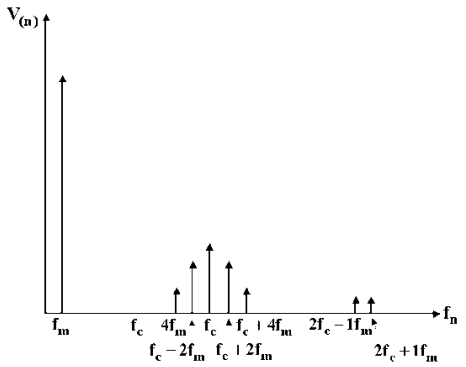


Fig3b. Harmonic spectrum
(Sine-triangle Comparison)

From Fig.3b it can be noted that the higher amplitude harmonics are centered around the carrier frequency and its side bands. So if the frequency of the triangle wave is very high compared to the sine wave (modulating wave) then the impedance offered to these harmonics from an inductive load will be higher and hence amplitude of these harmonic currents will reduce considerably with increase in the carrier wave frequency. But this will result in high switching frequency for the output chopped waveform. For high power applications an increase in switching frequency means increase in switching losses and decrease in efficiency. So, high switching frequency PWM are not used in high power applications, with two level inverters. The two-level inverters are widely used in low voltage, low power application. However, for high power, medium- and high- voltage applications, it suffers from the following disadvantages.

1. Harmonic distortion of the output voltage is high and hence filters will have to be used at the output in many applications, especially when the switching frequency is low.
2. The switching frequency has to be high to reduce the size of the filter. High switching frequency will cause increase in switching loss. It may be difficult to achieve high switching frequency in high voltage applications due to the device limitations.
3. Because of high frequency switching between two voltage levels, the dv/dt will be very high. This will result in doubling of voltages at the motor terminals due to the phenomenon of reflection.
4. Significant amount of conducted and radiated EMI will be generated and special filters will have to be provided in many applications to mitigate the harmful effects of EMI.
5. Two-level inverters generate substantial amount of common mode voltages that cause mechanical failure of the motor.
6. The voltage stress on the devices is high. In high voltage applications many devices will have to be connected in series which normally causes voltage sharing problems among the devices and additional circuitry will have to be provided for equalizing the voltages.The problems of the two-level VSI in high and medium voltage

applications, listed above, are either completely solved or mitigated to a great extent in multilevel power converters. The next section describes the concept of multilevel power conversion and the prominent topologies of multilevel converters

3. Multilevel inverters

Multilevel voltage source converters Multilevel power converters are being increasingly used for high power medium and high- voltage applications like high power AC drives, active power filters, reactive power compensation, HVDC transmission, FACTS devices etc [5]-[6]. The term 'level' means number of steps in the pole voltage waveform with respect to an internal reference point. Multilevel power converters have many significant advantages compared to the traditional two-level converters. Multilevel inverters are capable of producing output voltage with low harmonic distortion at reduced switching frequency. Since the switching is between smaller voltage levels, the voltage stress on semiconductor switches is reduced, in addition to the reduction in dv/dt. Low electromagnetic interference, reduced common mode voltage, higher efficiency etc. are the other advantages of the multilevel power converters compared to their two-level counterparts. By increasing the number of levels, nearly sinusoidal waveform can be obtained from a multilevel inverter and hence expensive and bulky filters can be avoided, in many applications. Figure.4 shows the schematic diagram of one leg of a three-level inverter along with the pole voltage waveform.

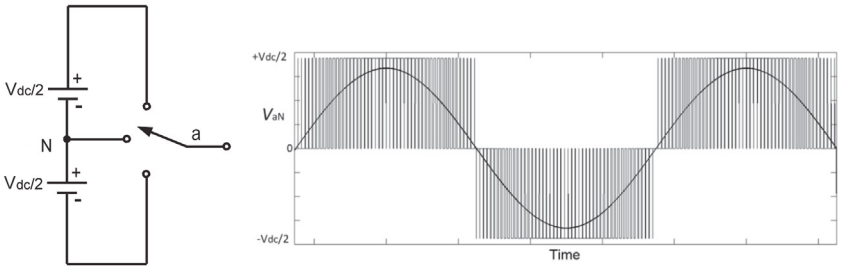


Fig.4a Schematic diagram of one leg of a 3-level VSI and Fig.4b the 3-level PWM output with reference waveform.

Fig.4a can be considered as a single pole 3-way switch which connects the pole to '3' different voltages depending on the position of the switch. It can be seen from Fig.4b that for the 3-level, there are 3 steps in the pole voltage waveform and the maximum instantaneous error between the desired sinusoidal voltage and the actual voltage is now reduced to half (Vdc/2) compared to the two-level inverter depicted in Fig.2a. This will significantly reduce the harmonic distortion thereby improving the quality of the output voltage. One leg of a general n-level inverter and the pole voltage waveform for n = 9 are shown in Fig5. It can be considered as a single pole 9 way switch which connects the inverter pole to '9' different voltage magnitudes. As the number of levels increases, the number of steps in the pole voltage waveform increases and the maximum

instantaneous error between the reference waveform and the actual waveform decreases resulting in drastic reduction in the harmonic distortion. A comparison of the pole voltage waveforms given in Fig-4b and 5b also reveals how the dv/dt reduces as the number of levels increases. In general, in an n-level inverter, the pole voltage can assume any one of the 'n' voltage levels as switching takes place. A number of multilevel converter topologies have been proposed, since the introduction of the concept of multilevel power conversion in late 1960's, [6]-[7].

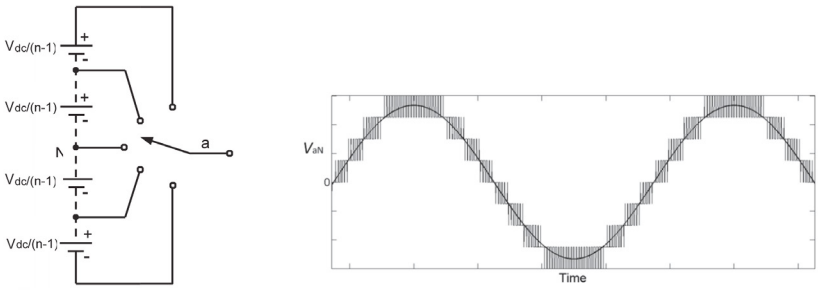


Fig.5a Schematic diagram of one leg of an n-level VSI and Fig.5b the PWM output with reference waveform (for n=9).

Among these, three converters namely the neutral point clamped (NPC) inverter, the flying capacitor (FC) inverter and the cascaded H-bridge (CHB) inverter are known as conventional multilevel converters. The three-level NPC topology proposed by Nabae, I. Takahashi, and H. Akagi, in 1981 [8] is one of the most popular multilevel voltage source inverters in the industry. The power circuit diagram of a three-level NPC is given in Fig.6

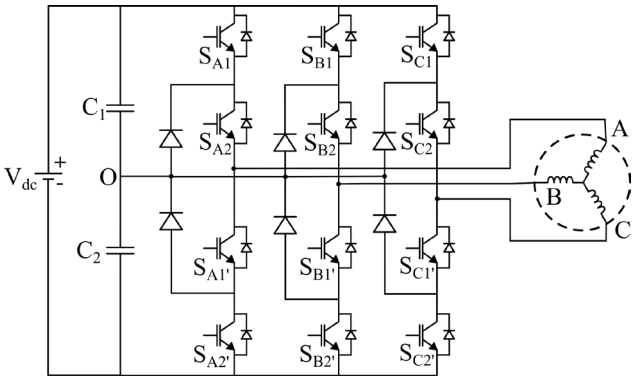


Fig.6 Power circuit diagram of a three-level NPC inverter

In this topology, the DC link voltage is split into a number of small voltage level using series connected capacitor banks. In the three-level NPC inverter shown in Figure-1.5, the middle point O of the two dc-link capacitors C1 and C2 is defined as the neutral-point. If Vdc is the DC link voltage, with respect to the neutral point 'O', the inverter pole voltage can assume three levels namely +Vdc/2, 0 and –Vdc/2, if C1 and C2 are selected in such a way that the voltage across them are equal. In addition to the extra active switches, the presence of two diodes in each inverter pole makes this topology different from the traditional two-level inverters. Since these diodes clamp the switch voltage to the capacitor voltages (Vdc/2 if the capacitor voltages are balanced), they are known as 'clamping diodes'. Thus compared to the two-level inverter, the maximum voltage stress on each switch is limited to half of the DC link voltage. The NPC topology can be extended to higher number of voltage levels at the output [9]-[10]. But as the voltage levels of the NPC topology is increased the power circuit complexity will also increase with the increasing levels and hence other than three level is not seriously considered for industrial applications.

The flying capacitor (FC) multilevel inverter, introduced by T.A.Meynad and H. Foch in the year 1992, is another well-established topology, in which the floating voltages across the capacitors are used for generating different voltage levels [11]. The basic concepts, modeling and analyses of this topology are given in [12]-[14]. A three-level flying capacitor inverter is shown in Fig.7.

The performance of this topology greatly depends on the balancing of the capacitor voltages, as the load current flows through the capacitors. PWM techniques for balancing the flying capacitor voltages are given in [15]-[17]. An analysis of the voltage balancing dynamics of a three-phase flying capacitor converter is presented in [16].

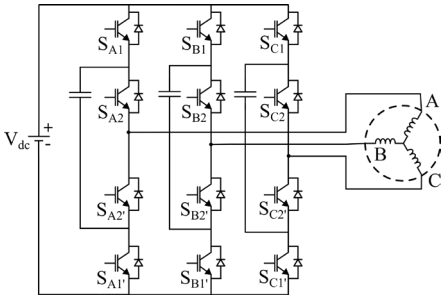


Fig.7. A three level flying capacitor topology

As the number of levels in voltage increases, the FC circuit becomes complex, due to the substantial increase in number of capacitors. A three phase n-level flying capacitor based multilevel inverter requires 3*(n-2) capacitors of unequal voltage ratings or

3*(n-1)*(n-2)/2 capacitors of voltage equal voltage ratings of Vdc/(n-1), where Vdc is the DC link voltage. A method to increase the number of voltage levels by changing the ratio of the capacitor voltages in flying capacitor topology is reported in [18]. In this scheme since the switching devices have to withstand asymmetric voltages it is known as asymmetric flying capacitor inverter. However, in asymmetric flying capacitor inverter higher number of levels cannot be achieved in the entire modulation range due to the difficulty in balancing the capacitor voltages. Another disadvantage of asymmetric FC topology is that the number of voltage levels that can be achieved with capacitor voltage balancing depends on operating power factor. Hence this scheme is suitable only for certain applications.

Cascaded H-bridge inverter (CHB) The cascaded H-bridge (CHB) multilevel converter, which employs series connection of H-bridge cells fed from isolated DC voltage sources, is another topology widely used in the industry. A five-level cascaded H-bridge inverter is shown in Figure-1.9.

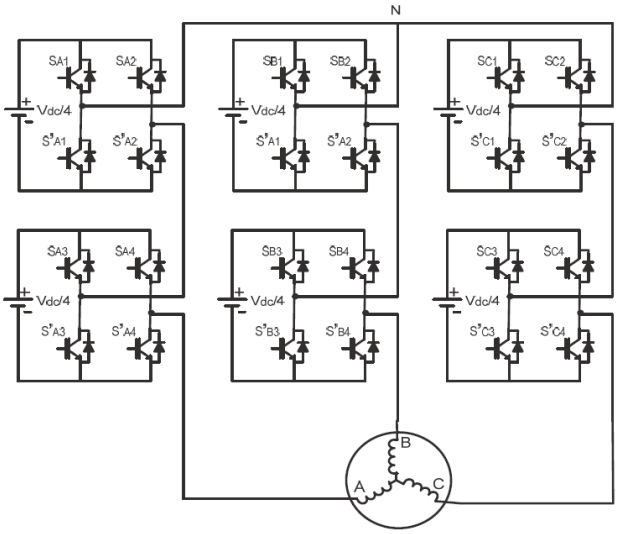


Fig.8 A five level cascaded H-bridge topology

The CHB topology is preferred in many high voltage applications due to its modular structure and simple control schemes [19]-[22]. This topology is free from issues like capacitor voltage balancing. A major limitation of this topology is the requirement of multiple DC voltage sources, as each H-bridge cell requires a DC source. This topology is considered well suited for applications like PV systems, where obtaining multiple DC sources is not a constraint [23] or applications without active power conversion, like STATCOM [24]-[25]. However, when conversion of real power is required, the difficulty in obtaining so many DC sources may preclude the use of the CHB inverters, in many applications.

4. Hybrid Multilevel Inverter Topologies

Hybrid multilevel inverter topologies can be developed by combining conventional (two level inverter, NPC, FC and CHB) topologies [26]. In Fig.9a, a hybrid five level inverter is formed by cascading a three level NPC with a H bridge fed by a charged capacitor.

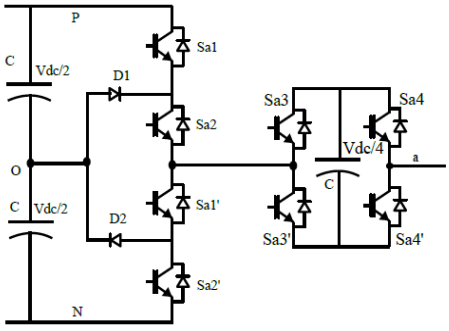


Fig.9a.A hybrid five level inverter topology by cascading three level NPC inverter and a CHB module

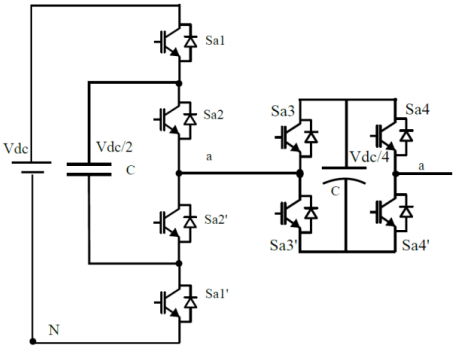


Fig.9b. A hybrid five level inverter topology by cascading a flying capacitor topology and a CHB module

This topology has the advantage of both NPC and CHB inverter topologies as it requires less number of clamping diodes compared to a five level NPC and less number of isolated power supply compared to a five level CHB inverter. In Fig.9b the NPC is replaced with a Flying capacitor topology. The advantage of this topology is the single DC supply requirement [27]. The three phase configuration of the above hybrid five level inverter

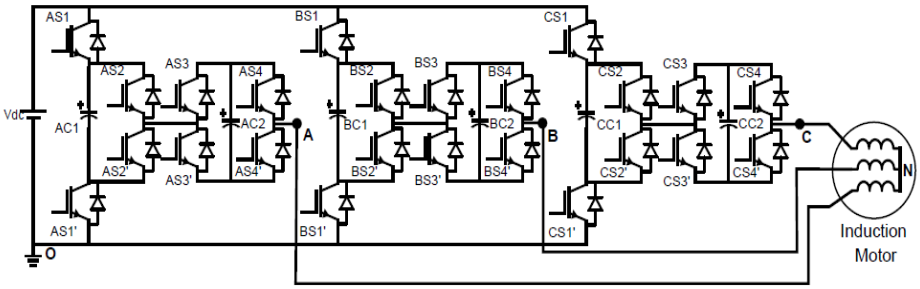


Fig.10a. Three phase circuit of hybrid five level inverter topology by cascading a flying capacitor topology and a CHB module is shown in Fig.10a.

The five pole voltage levels are 0, VDC/4, VDC/2, 3VDC/4, and VDC. All these five voltage levels are generated by the DC link along with the charged capacitor in each phase. These capacitor voltages can be controlled around the nominal value of VDC/4 using the switching state redundancies in each PWM cycle. A typical example is shown in Fig.10b and Fig.10 c below.

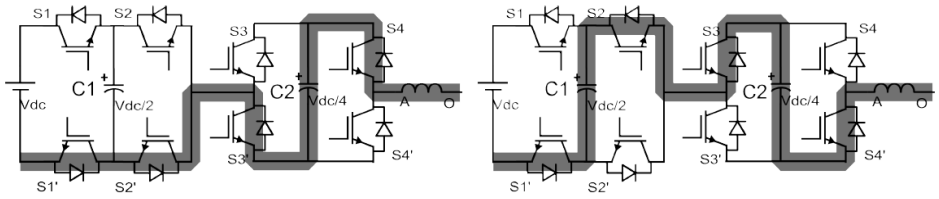


Fig.10b. The Vdc/4 capacitor voltage control

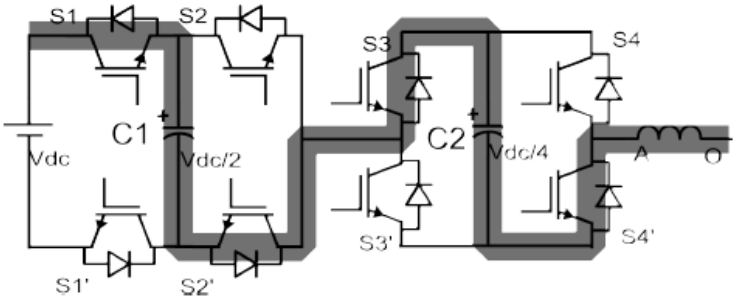


Fig.10b. The Vdc/2 capacitor voltage control

The out phase voltage, current and the capacitor voltages from an experimental results are shown in Fig.10c and 10d below, and it can be seen that the capacitors are tightly controlled using the switching state redundancies.

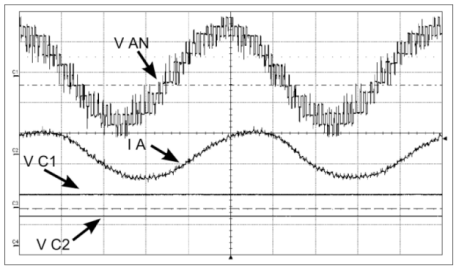


Fig.10c. The motor phase voltage, current and capacitor voltages- steady state operation

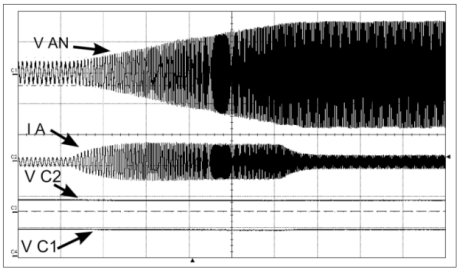


Fig.10d. The motor phase voltage, current and capacitor voltage during transient condition

The same Power circuit configuration of Fig.10a can be repeated at the DC source side and the power can be directly taken from the grid with appropriate control for unity power factor operation at the front end side. The schematic of this unity power factor control from the frontend using the back to back five level power converter scheme is shown in Fig.10e below. From fig 10e it can be noted that the DC link voltage is replaced by a capacitor. This is for generating the magnetising current for the motor and the real part of the power is directly taken from the grid. So with this back to back topology we have eliminated all the DC voltage requirements for generating a multilevel topology and the power is directly taken from the mains.

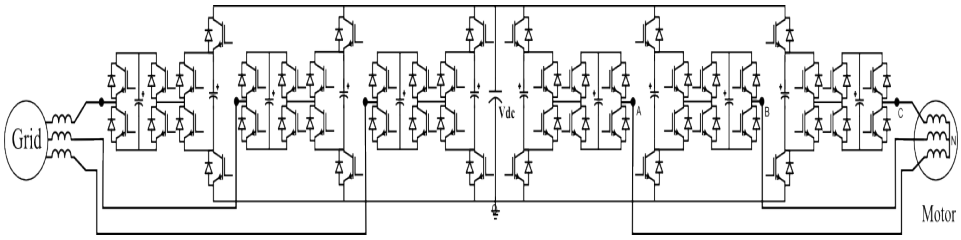


Fig.10e. Five level back to back power converter for Induction motor drive

In this back to back topology all the DC power supplies are replaced by charged capacitors, which only gives the reactive power and regeneration of the power from the load side to the grids side is also possible in such a scheme. The motor phase voltage, current and the grid side voltage and current during a steady state operation is shown in Fig. 10f , below.

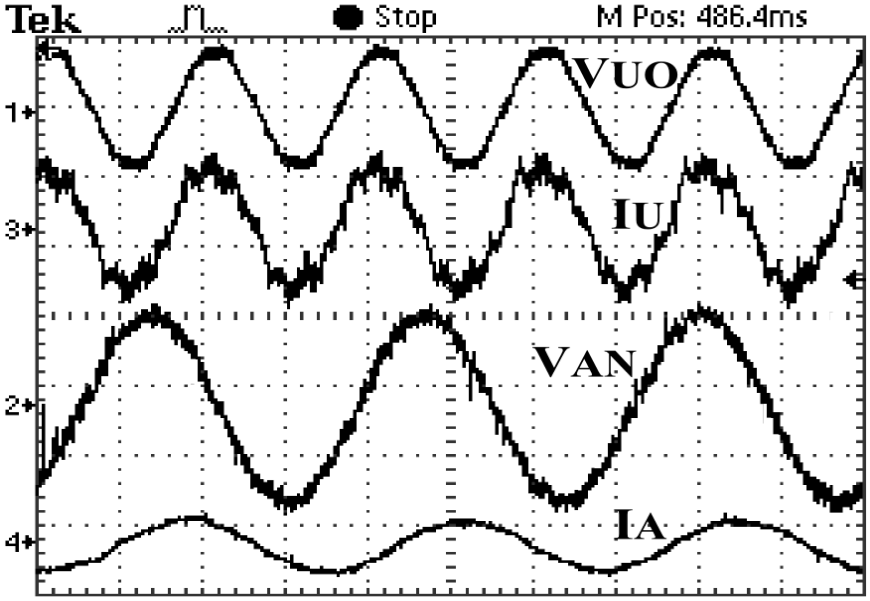


Fig.10f. Grid voltage and current with unity power factor and the motor phase voltage and current with a lagging power factor

The hybrid topology by cascading the flying capacitor topology with an H bridge can be further extended for generating more number of levels by cascading more number of H bridges. [28]–[29].

Fig.10.g and Fig10h shows the power schematic of hybrid nine level and seventeen level inverter schemes for drives applications.

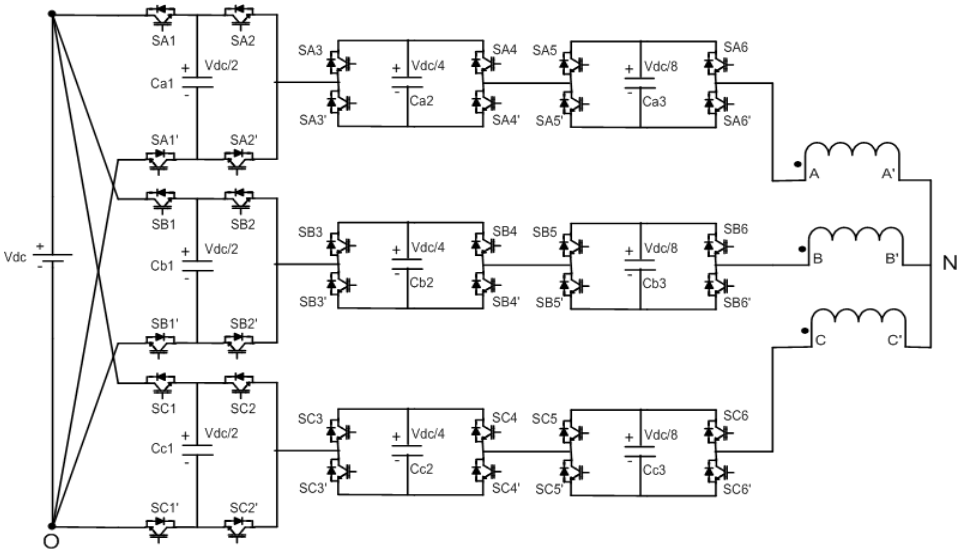


Fig.10g. Three phase circuit of hybrid nine level inverter Nine pole voltage levels are -VDC/2, -3VDC/8, -2VDC/8, -VDC/8, 0, +VDC/8, +2VDC/8, +3VDC/8 and +VDC/2.

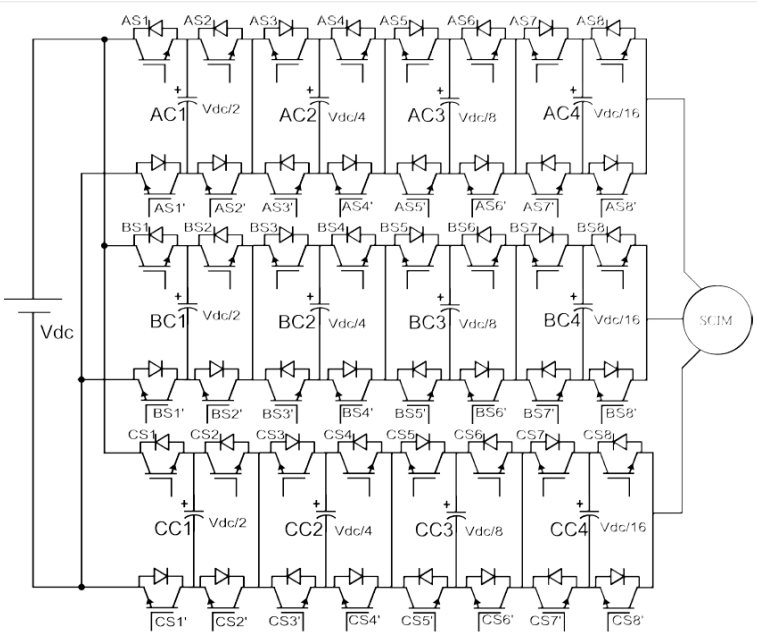


Fig.10h. Three phase circuit of hybrid seventeen level inverter The seventeen pole voltage levels are-0, VDC/16, VDC/8,3VDC/16, VDC/4, 5VDC/16, 3VDC/8, 7VDC/16, VDC/2, 9VDC/16, 5VDC/8, 11VDC/16, 3VDC/4, 13VDC/16, 7VDC/8, 15VDC/16,VDC,

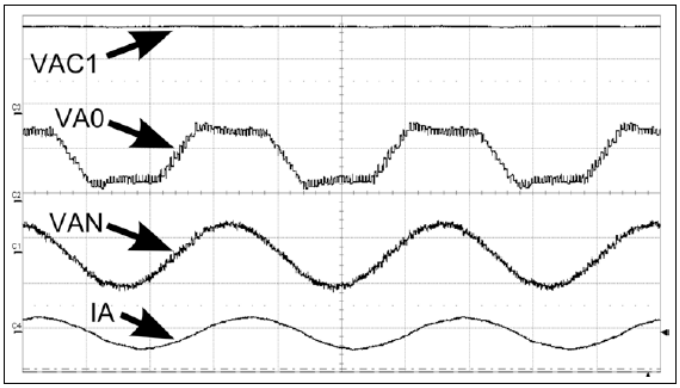


Fig.10i. Machine phase voltage, phase current and pole voltages of the hybrid seventeen level inverter fed drive.

The Phase voltage, phase current and the capacitor voltages for a seventeen level inverter fed induction motor drive is shown in Fig.10i. It can be noted that the phase voltage profile (VAN) is very close to a sine wave. This means as the number of pole voltage levels increases correspondingly the output phase voltage profile become very close to a sinusoidal wave. But it can be noted form Fig.10.h that as the number of cascaded H bridges increases, the value of the capacitor voltage feeding these bridges becomes lesser and lesser and in the end it will become closer to the device drops. So cascading more H bridges to increase the pole voltage levels is not a viable solution. This can be solved with stacking more basic inverter modules along with cascading.

5. Stacked Multilevel Inverter Topologies

A nine level inverter scheme with stacking the two basic five level structure of Fig.9b is explained below [30].

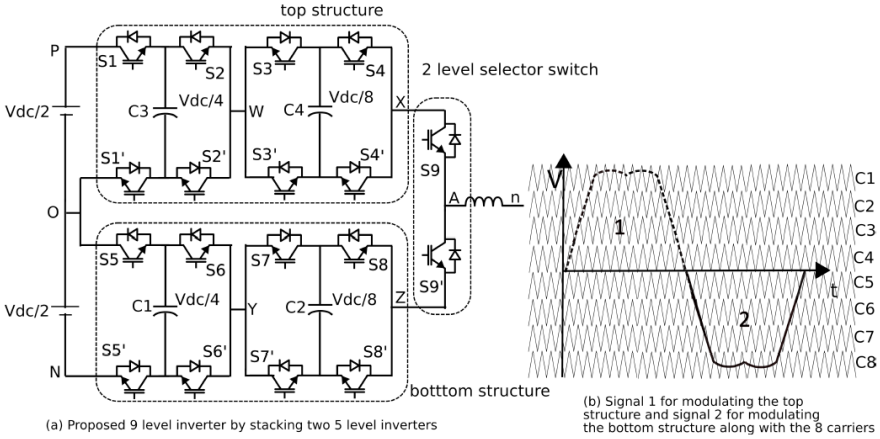


Fig.11a. shows the Power circuit for the proposed stacked nine-level inverter and its modulating signal for phase-A. The nine levels are 0, Vdc/8, 2Vdc/8, 3Vdc/8, 4Vdc/8, 5Vdc/8, 6Vdc/8, 7Vdc/8, Vdc

From the modulating waveform(Fig.11a) shown above, it can be noted that the top five level structure is selected for PWM control, when the modulating wave is positive (switch S9 is ON) and in the negative cycle of the modulating wave the bottom structure is selected(switch S9' is ON).

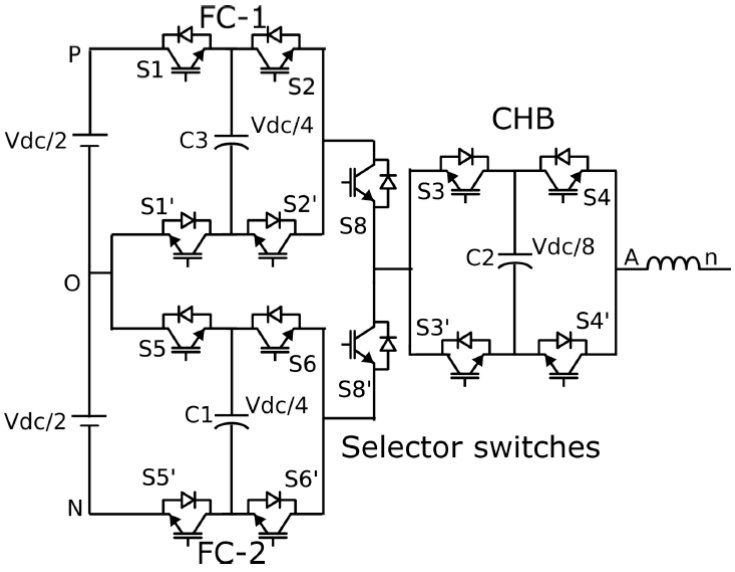


Fig.11b. Modified power circuit to reduce number of switches for the proposed stacked nine-level inverter topology for phase-A

Fig11a can be further modified to reduce the number of device count, by making the cascading H bridge cell common to both the stacked cells, as shown in Fig.11b. The same structure will produce all the nine levels for the phase voltages, as the fig 11a., with reduced H bridge cells.

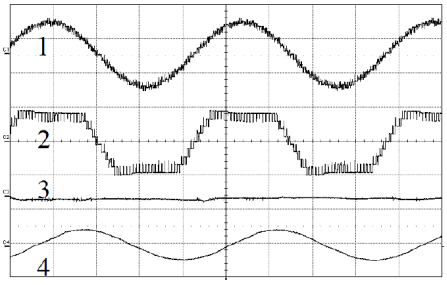


Fig.11d. 45 Hz operation, x-axis: 5ms/div. y-axis 1) VAn: 100V/div, 2) VAO: 100V/div; 3) _Vc3: 5V/div 4) IA: 2A/div

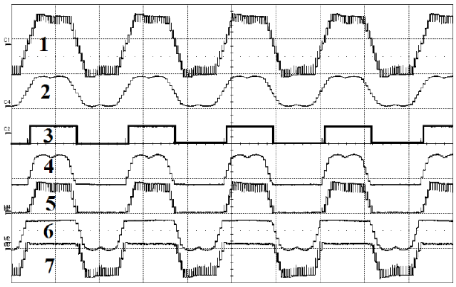


Fig.11e. Modulating signals and the generated pole voltages by each of the stacked cells45 Hz operation. 1) VAO: 100V/div, 3) Gating signal to selector switch: 50V/div, 5) VXO: 100V/div, 7) VZ0: 100V/div. x-axis: 10ms/div.

Fig.11d shows the phase voltage, pole voltage, capacitor voltage and the phase current wave form for 45Hz operation and Fig.11e shows the Pole voltage waveform and the modulating wave forms along with the selector switch gating waveform and the part of the modulating wave for the upper part and lower part of the stacked cells. It can be noted from Fig.11e that the during the upper part of the modulating waveform the upper cell only works and for the lower part of the modulating wave the lower cell only works. This way each module works only for fifty percent of the fundamental cycle there by reducing the switching losses and increasing the efficiency of the overall inverter system. The selector switch works with fundamental frequency. The proposed stacking concept can also be further extended for a 49 level structure by cascading the previously mentioned 17 level structure of Fig.10h. By stacking three such cells a 49 level inverter structure can be realised. Here also the H bridges can be made common for all the three main cells by a selector by appropriately cascading the H bridges after the three way selector switch [31]. The proposed 49 level structure with reduced H bridge cells for the Phase-A are shown in Fig. 12a.

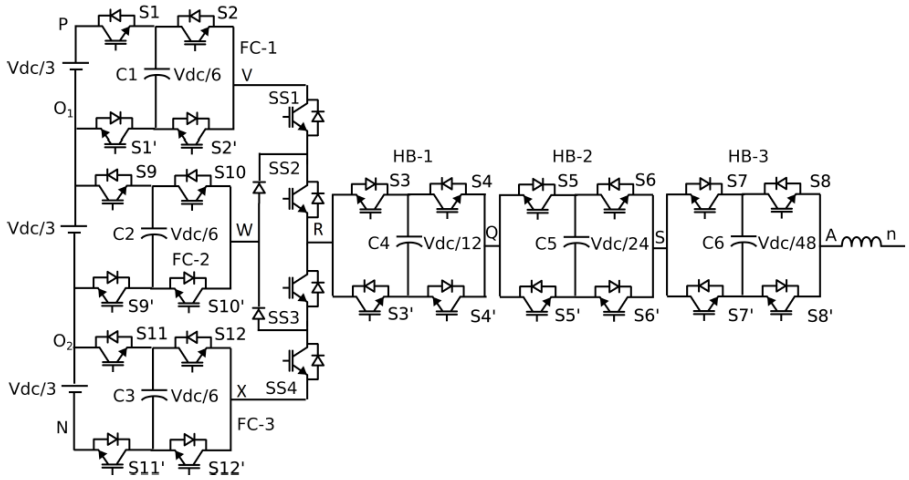


Fig.12a.Reduced device count 49-level inverter by making the CHBs common to the stacked FCs for phase-A

Fig.12b below shows the typical phase voltage, phase current and capacitor voltage for a steady state operation form an experimental set up.

(VAN), 3) Capacitor voltage (Vc1), 4) Phase currents (Ia) It can be noted that with more number of levels the output phase voltage will be very close to a sinusoid. The fig.12a can be further modified for a lesser DC Voltage requirement by reconfiguring symmetrical six phase induction machine with the same power rating, as a normal there phase machine [32]. The schematic of a six phase machine phase winding diagram are shown in Fig12c and Fig12d.

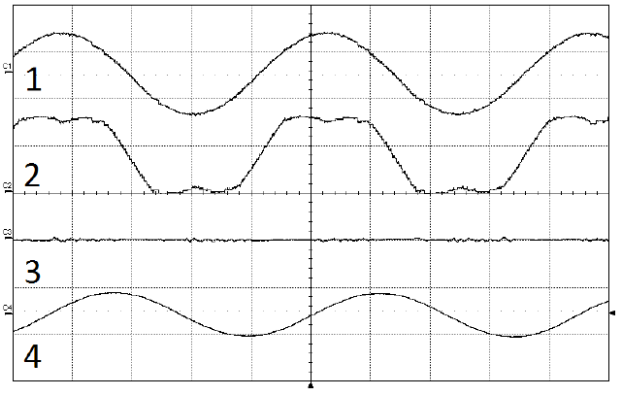


Fig.12b. Steady state results. 1) Motor Phase voltage (VAn), 2) Inverter pole voltage

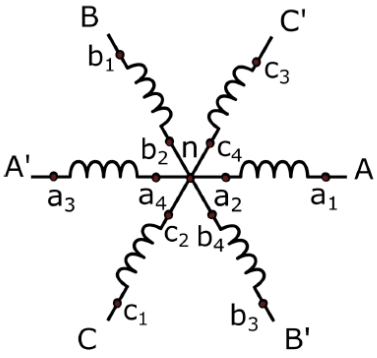


Fig.12c. A symmetric six phase winding

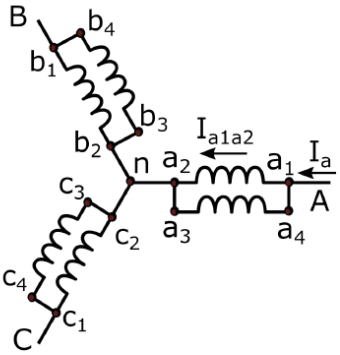


Fig12d. Reconfiguring as a three phase winding.

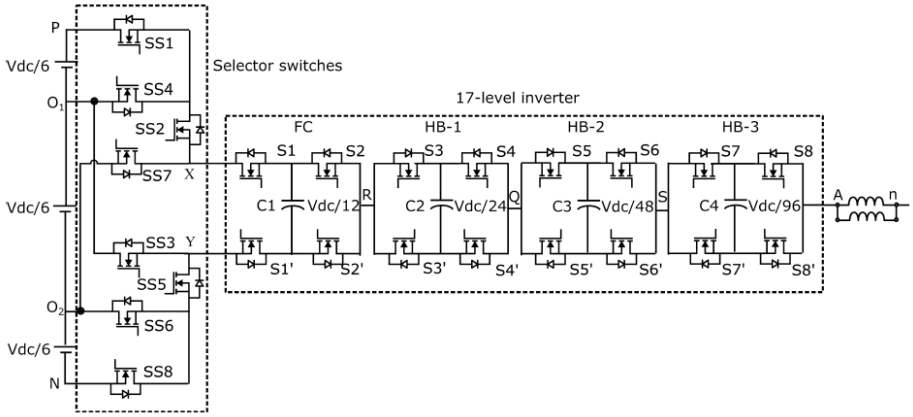


Fig.12e.Reduced device count stacked 49-level inverter topology for phase 'A' by cascading an FC with three CHBs and stacking them using selector switches

By using the winding pattern of Fig.12d, the DC link requirement for the inverter configuration of Fig12a can be further reduced and the inverter can be directly fed from batteries for EV applications. The same configuration can also be improved with less number of devices by cascading the part of the stacked flying capacitor cells and make it common to all the three stacked main power cells, as shown in Fig.12e, below. The three DC sources can be reduced to Vdc/6 (instead of Vdc/3) if a six phase IM is used in a three phase winding configuration by connecting the 180 deg opposite windings in parallel configuration with appropriate polarity as shown in Fig.12d. This will reduce the DC link voltage requirement at front end because, for the same power output from a three phase IM and a six phase IM, a six phase machine needs only half the DC link voltage.

6. Voltage space vector structure of a three phase inverter

Table 1 shows the different switching states which the 2-level inverter (Fig.1) can take. There are 8 possibilities as shown in the table. As already mentioned, the top and bottom switch in a leg always operate in a complimentary fashion. '1' indicates top switch in a phase is ON and '0' indicates top switch is OFF. Space vector modulation, unlike a sinusoidal PWM, considers the three phases as one entity called as the space vector. A space vector transformation is defined as in equation 1.1. When the operation of the inverter is 3-phase balanced, the phase voltages add up to zero and therefore it is possible to transform the 3-phase quantities to equivalent 2-phase quantities as given in eqn.1. Using this transformation, the voltage space vector corresponding to each switching state can be plotted as shown in Fig.13.

$$V_3 = V_{ao} + V_{bo} + V_{co} \tag{1}$$

Table-1. Inverter switching state combinations, pole voltages and voltage space-vectors

Space Vector	Inverter state (a,b,c)	Pole voltages (v)			Voltage space vector (p.u, V_{dc})
		V_{ao}	V_{bo}	V_{co}	
V_0	(000)	0	0	0	0
V_1	(100)	V_{dc}	0	0	$1\angle 0°$
V_2	(110)	V_{dc}	V_{dc}	0	$1\angle 60°$
V_3	(010)	0	V_{dc}	0	$1\angle 120°$
V_4	(011)	0	V_{dc}	V_{dc}	$1\angle 180°$
V_5	(001)	0	0	V_{dc}	$1\angle 240°$
V_6	(101)	V_{dc}	0	V_{dc}	$1\angle 300°$
V_7	(111)	V_{dc}	V_{dc}	V_{dc}	0

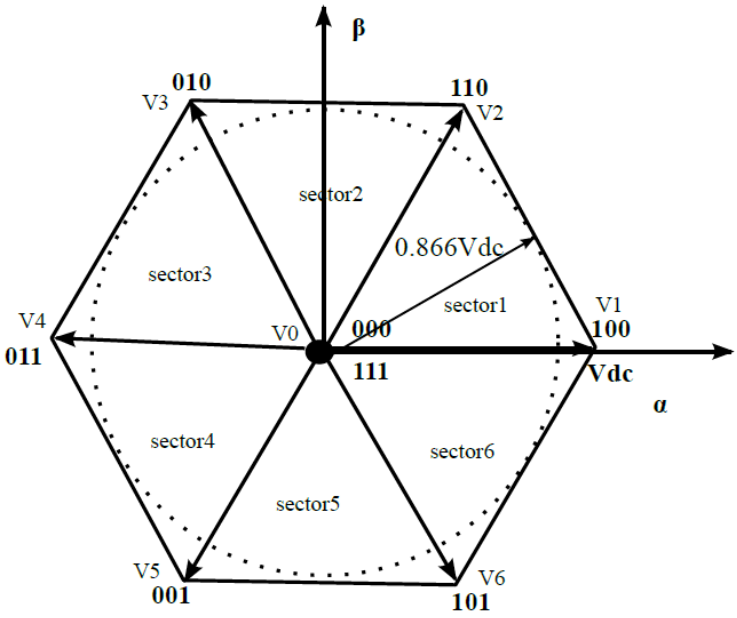


Fig.13a. Voltage space vector diagram for the 2-level inverter

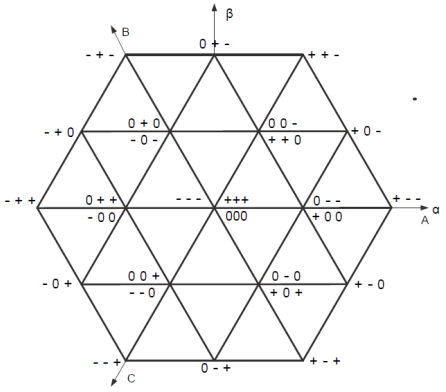


Fig13b. Three level inverter- voltage space vector structure

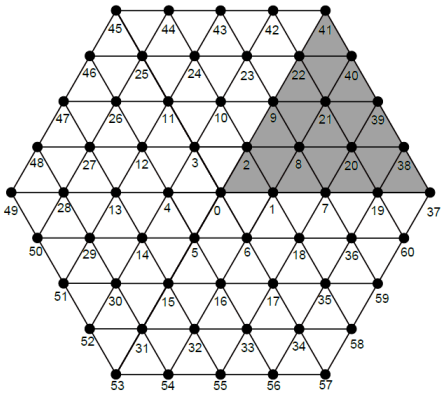


Fig13c. Five level inverter- voltage space vector structure

Fig 13 shows the voltage space vector structure of a two level three phase inverter. It can be noted that all the active space vectors (Table-1) are placed at the vertices of a hexagon and the Zero voltage vectors at the centre of the hexagon. The hexagonal structure is further divided in six equilateral triangles. For a machine to be excited with a sinusoidal voltage and current, we need a circular voltage space vector structure. An

average circular voltage space vector structure can be achieved by PWM techniques Here the reference circular voltage space vector is sampled at high frequency and the triangular sector is first identified in which triangular sector the reference vector lies. Then the sampled vector is generated in a switched average(using volt-sec balance, in a sampling period) way by switching between the vertices of the triangular sector. For example in sector-1 the vertices, V1, V2 and V0 are switched for T1, T2 and T0 period such that T1+T2+T0=Ts.

In multilevel inverters the triangular sector will be further divided into small triangles and the size and the triangular size depends on the number pole voltage levels.

From fig13a, 13b and 13c, it can be noted that for the same radius of the polygon depends on the Vdc link amplitude), the maximum radius of the circular trajectory that can be inscribed within the hexagonal voltage space vector structure is 0.866 Vdc (Fig13a),resulting in a maximum phase peak fundamental of 0.577 Vdc for the motor phase voltage(limit of the linear modulation range). This is the limit of the linear modulation range. But the circular radius can be further increased (over modulation range) to get a maximum phase peak fundamental of 0.637 Vdc where the each inverter leg will operate in square wave mode (inverter six step mode operation) as in Fig2a. In voltage space vector sense the PWM operation will take the voltage space vector along the vertices of the hexagon where each vertex will be switched for sixty degree in a fundamental cycle of PWM operation of the inverter (Fig.13d). As the fundamental amplitude is increased above the linear modulation range, the low order harmonics will start appearing in the motor phase voltages as shown in Fig13e, below.

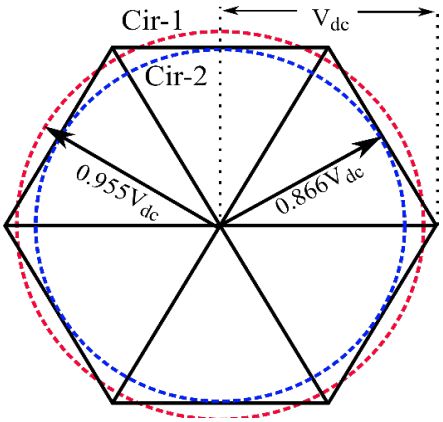


Fig13d Space Vector Structure generated by 2-Level inverter showing the extreme modulation range at six step mod operation

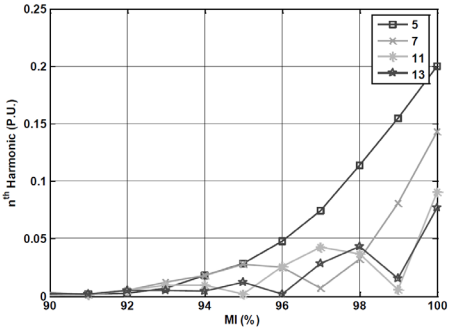


Fig.13e.Harmonic components in the output phase voltage in over modulation region

7. Increasing the linear modulation range without the presence of low order harmonics

In a multilevel structure such as the five level scheme a boost in the pole voltage level is possible with addition of a charged capacitor voltage over the Vdc link voltage of Vdc [33]. For example if we can generate Vdc+Vdc/4= 5vdc/4in a five level inverter, the resulting space vector structure will be six level instead of five level, as shown in Fig13f, below. Fig13g shows the circular voltage reference vector trajectory at the extreme modulation range where the phase peak fundamental of the motor phase voltage is 0.637Vdc. In Fig.13g Up to 5th Level, the charging and discharging redundancy are available for all the capacitors. But for the

space vector locations at 6th level generated by boosting the DC-link voltage by a charged capacitor of voltage Vdc/4, the capacitor will start discharging when the vector locations at the level 6 are used for PWM operation. But this can be balanced in PWM cycle by using the switching state redundancies at the fifth layer. This is possible because PWM timing in a sector for vectors forming the triangle from the fifth layer is more than that for the vector locations in sixth layer (Fig.13.g). This can be proved form the vector timing equations in a sampling interval shown in eqn.2

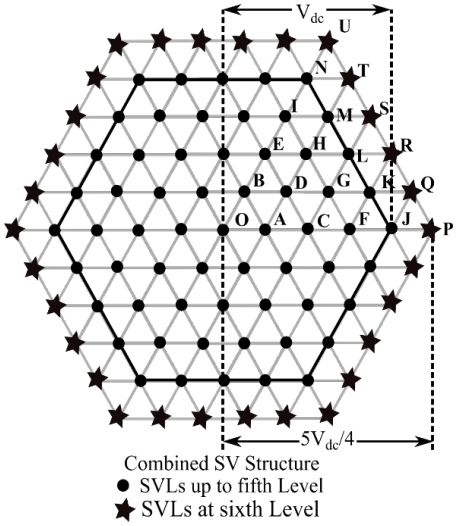


Fig13f. Six level space vector structure

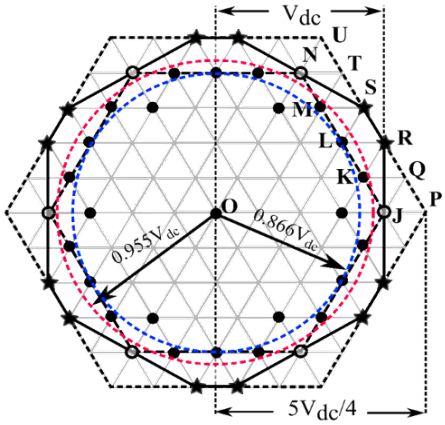


Fig13g.Refrence voltage vector trajectory at the extreme modulation range

$\mathbf{V_r} \angle 30^{*}T_s = \mathbf{OL}^{*}T_0 + \mathbf{OR}^{*}T_1 + \mathbf{OS}^{*}T_2$; $T_0 = 0.59T_s$; $T_1 = 0.206T_s$; $T_2 = 0.204T_s$

So, Time $\mathbf{T_0}$ is **greater than** $\mathbf{T_1 + T_2}$, $T_0 + T_1 + T_2 = T_S$ (sampling Time) (2)

- For extended modulation range, by applying SV **OQ** machine phase voltage (A-phase) will exceed by 12.5%.

- This can be avoided by modifying the extreme SV trajectory (shown by bold black line) and selecting vectors from this trajectory for PWM control.
- The PWM timings at the modified SV locations for operation with modulation index more than 0.577 can be obtained by timing calculation, as before presented in eqn.2

The power circuit for the proposed scheme is shown in Fig.13h below [33]

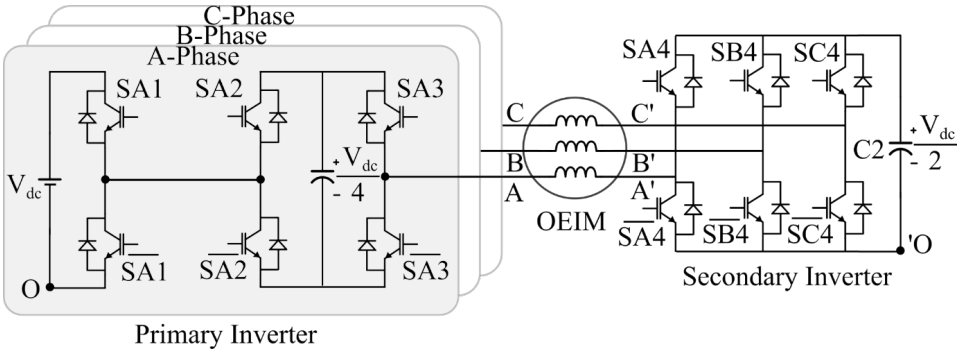


Fig.13h. The proposed multilevel power circuit schematic for extending the linear modulation range

An open-end winding induction motor drive scheme is selected for this drive configuration, where the neutral is open and fed from another two level inverter from other side of the machine [33]. The motor phase voltage waveforms in the extended linear modulation range (for the proposed scheme) and from the conventional over modulation region are presented in Fig.13i and Fig.13j, below.

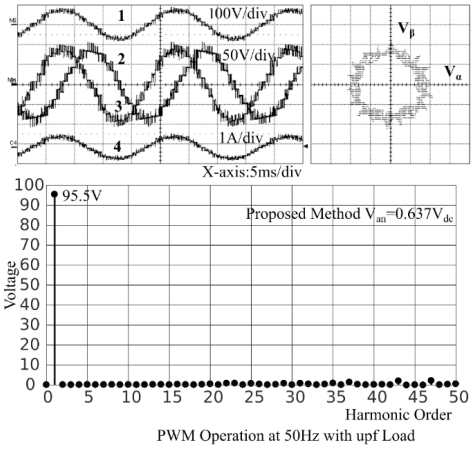


Fig13i. Motor phase voltage and current at the extended linear modulation range (base speed operation)

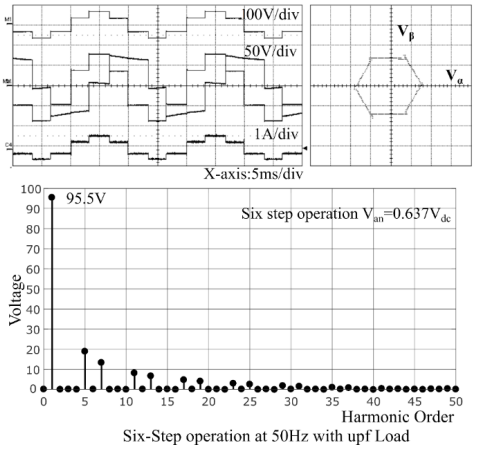


Fig.13j. Motor phase voltage and current from a Conventional inverter at six step mode operation (base speed)

From Fig.13i, it can be noted that the same maximum phase peak fundamental can be achieved with the proposed technique to increase the linear modulation range without the presence of low order harmonics, when compared to the conventional method as presented in Fig.13j.

But another very interesting technique is reported in literature to increase the linear modulation range of a variable speed drive system, with the suppression of low order harmonics, for the full modulation range [34]–[36]. These are mainly called polygonal voltage space vector based inverters with the polygonal voltage vector sides more than six, when compared to the conventional hexagonal structure.

8.Three phase inverter PWM technique with polygonal voltage vectors

A 12isded (dodecagonal) voltage space vector structure is possible by feeding an open-end winding induction machine form two inverters fed by asymmetrical voltages as shown in Fig.14a and 14b [34]. Since the two inverter control are independent of each other a selective vector combination from both the inverter will result in a 12sided polygonal vector structure (Fig.14b). The output phase voltage during the extreme 12 step mode is shown in Fig.14.c. The harmonic analysis of this waveform will show that all the 5th and 7th order harmonics (6m±1,m = odd) are absent in the proposed 12dodecagonal scheme. The secondary DC voltage can also be replaced with a charged capacitor with appropriate magnitude and angle.

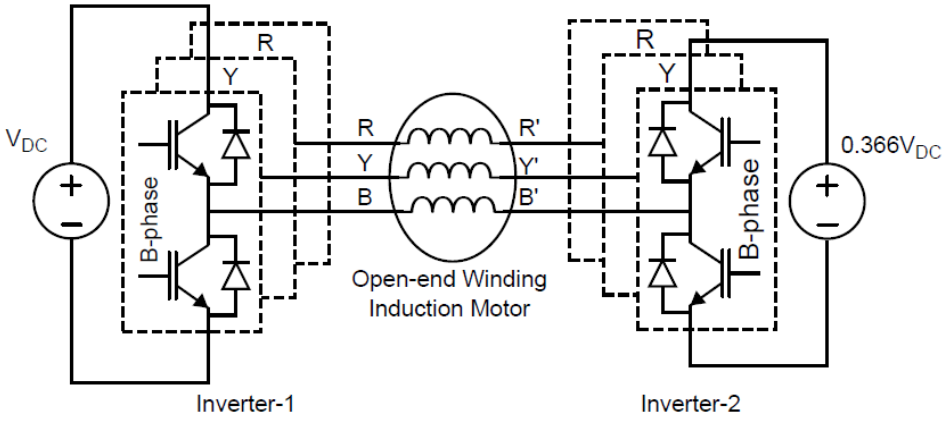


Fig.14a. Power circuit for generating a 12 sided polygonal voltage space vector structure

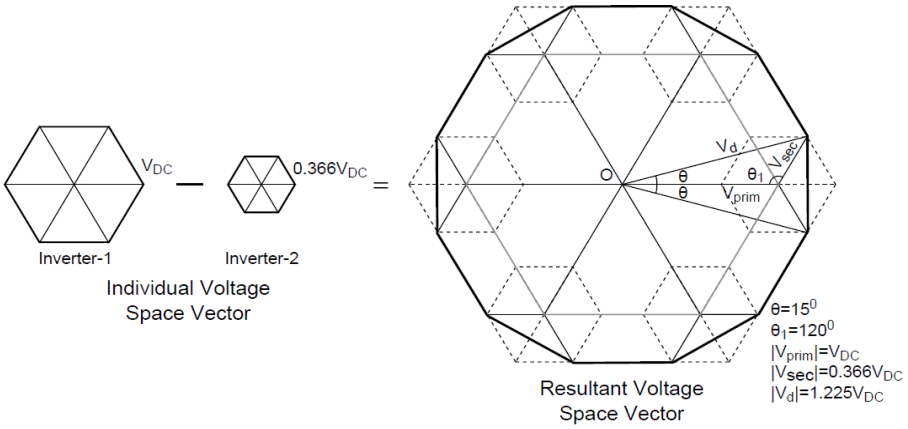


Fig.14b. Generation of the 12sided polygonal voltage vectors from inverters feeding an open-end winding induction motor drive with asymmetrical voltages

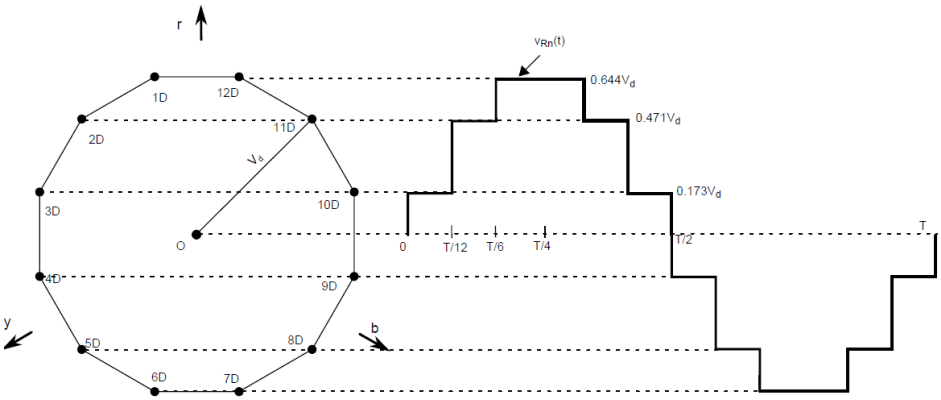


Fig14c. Twelve step phase voltage waveform for extreme stepped operation with dodecagonal voltage space vector

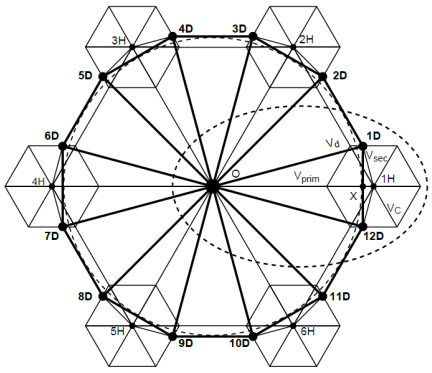


Fig14d. Formation of a switched average12sided vector by feeding the second inverter with a charged capacitor.

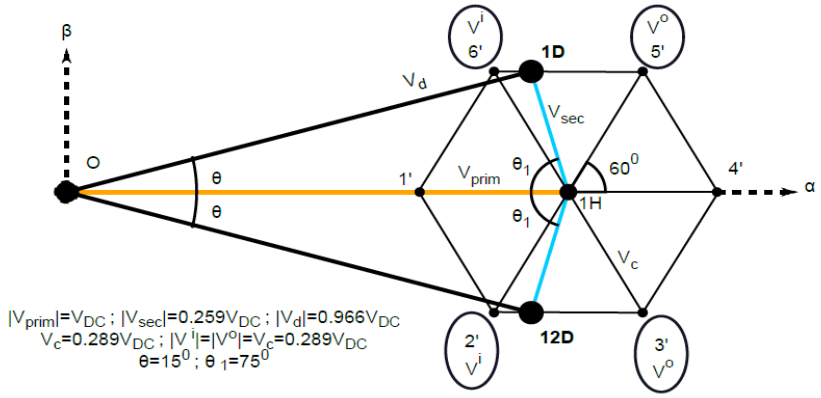


Fig.14e. Generation and superimposition of the switched average vector from the secondary side, with the primary inverter vector

So that during PWM operation the main inverter will feed the real power and the secondary inverter will feed the reactive power so that the fifth and seventh harmonics can be eliminated from the primary inverter pole voltages to realise the 12sided polygon [34].

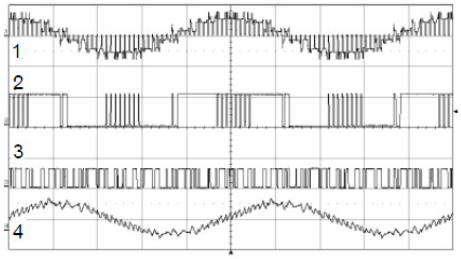


Fig14f. 40Hz operation. 1) phasevoltage, 2) Inverter-1 pole voltage, 3) inverter-2 pole voltage, 4) motor phase current

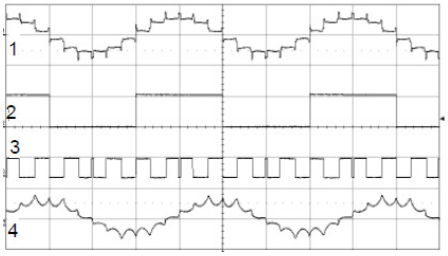


Fig14g. 50Hz operation. 1)phasevoltage, 2) Inverter-1 pole voltage, 3) inverter-2 pole voltage,4) motor phase current

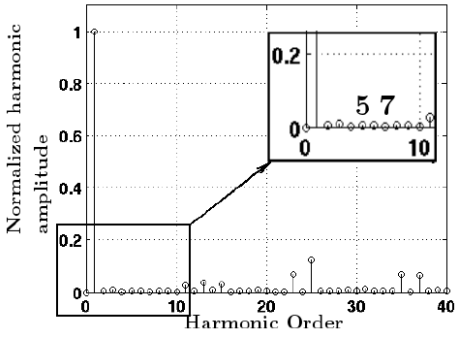


Fig.14h.Harmonic spectrum-40Hz operation

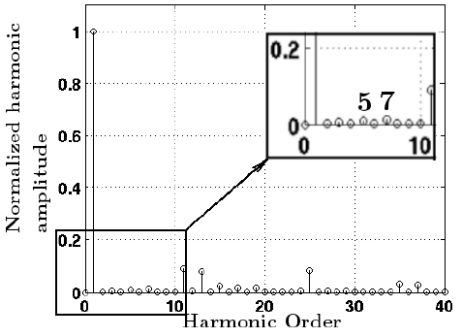


Fig.14i.Harmonic spectrum-50Hz operation

It can be noted that the drive can go up to the square wave mode operation for the inverter-1 and phase voltage has a 12-step profile with the absence all the 5th and 7th order harmonics. The relative harmonic amplitudes are shown in Fig.14h and Fig.14i, for the 40Hz and 50Hz operation, respectively.

So with the PWM operation with a 12sded polygon will result in the absence of all the 5th and 7th order harmonics throughout the modulation range up to base speed of 50Hz operation where the inverter-1 will be running with the pole voltages in square wave mode operation. Instead of two 2-level inverters (Fig14a),if we use two the 3-level inverter structures, then the resultant space vector combination will generate a multilevel 12isded voltage space vector structure as shown in Fig14j, below.

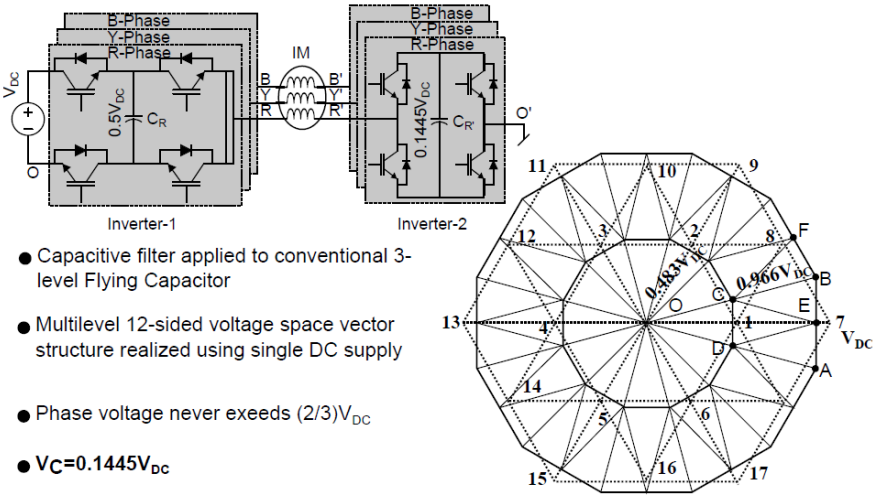


Fig14j. The three level power circuit combination and the resultant multilevel 12sided voltage space vector structure

The motor phase voltage and current from the above power circuit combination is shown in Fig.14k and Fig.14l for 40Hz and 50Hz operation.

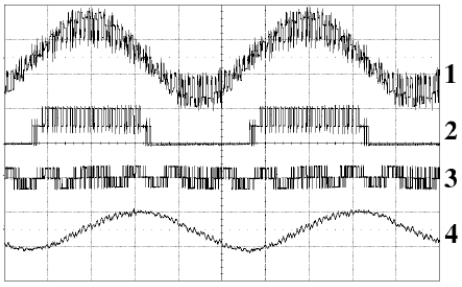


Fig14k. 40Hz operation.: 1) phasevoltage, 2) Inverter-1 pole voltage, 3) inverter-2 pole voltage, 4) motor phasecurrent

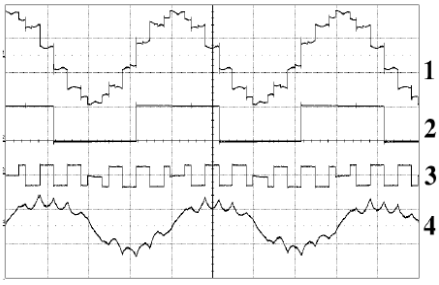


Fig14l. 50Hz operation: 1) phasevoltage, 2) Inverter-1 pole voltage, 3) inverter-2 pole voltage, 4) motor phasecurrent

Since the PWM is done using voltage vectors placed at the 12 sided structure her also all the fifth and seventh harmonics will be absent throughout the modulation range up to square wave mode operation for the Inverter-1. The same inverter concept can be extended to multilevel 18sided, 24 sided and 30sided structures as explained below, for achieving nearly sinusoidal phase voltage waveform with less switching for the main real power delivering inverter-1. Here the secondary inverter acting as a switched capacitive filter for suppressing low order harmonics up to 13th suppression for the 18-sided scheme [35], 19th order suppression for the 24 sided scheme[36]. In all these schemes the main inverter will be delivering the real power and the capacitor fed secondary inverter will act as a switched capacitive filter for the low order harmonic suppression, throughout the modulation range.

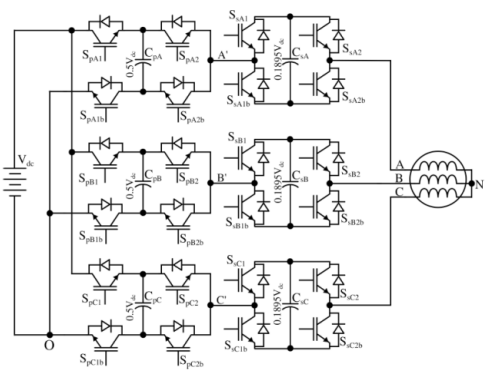


Fig15a. Powercircuit for the 18sided polygon

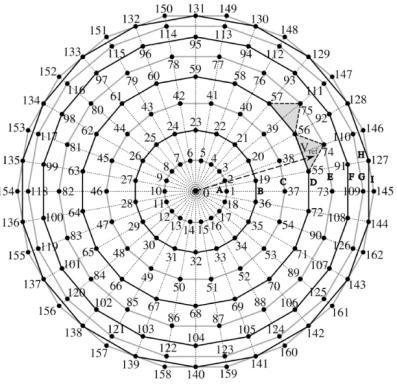


Fig.15b. nine concentric 18sided polygon

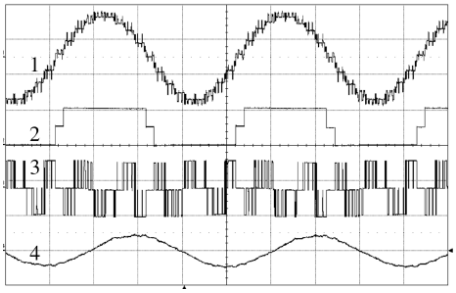


Fig.15c. 40Hz operation – multilevel 18sided polygonal based PWM

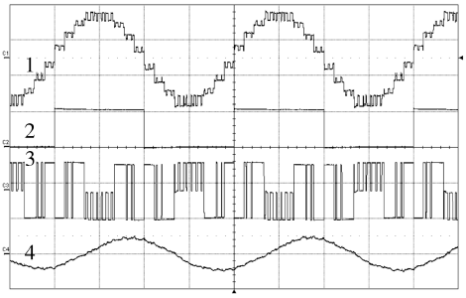


Fig.15d. 50Hz operation – multilevel 18sided polygonal based PWM

Fig15a shows the schematic of the cascaded flying capacitor topology with capacitor fed H-bride for the multilevel 18-sided polygon generation. Fig15b shows the nine concentric 18sided polygonal voltage vector structure from this inverter scheme [35].

The experimental results are shown in Fig.15c and Fig 15d, for the 40Hz and 50Hz operation, respectively.

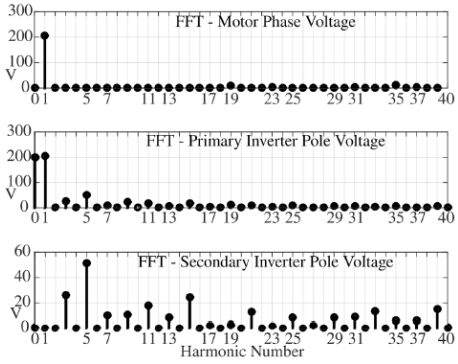


Fig.15e.Harmonic spectrum-40Hz operation

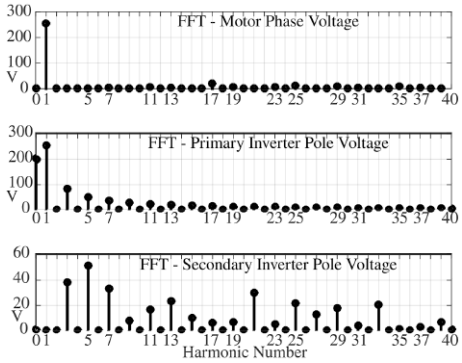


Fig.15f.Harmonic spectrum-50Hz operation

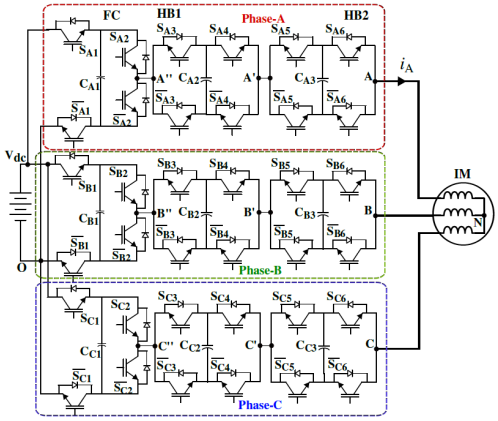


Fig16a.Powercircuit for the 24 sided polygon

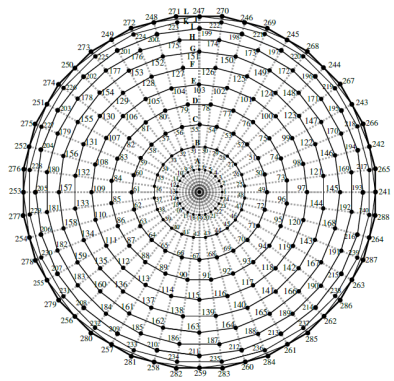


Fig.16b. twelve concentric 24sided polygon

In Fig.15c and Fg.15d the Inverter pole voltage waveform (trace-2) from the primary inverter is in quasi square wave form for the 40Hz operation and a square wave in 50Hz operation. All the inverter switchings (trace-2) are transferred to the secondary inverter acting as a switched capacitive filter, eliminating all the low order harmonics, as shown in Fig.15e and 15f, from the phase voltages (trace-1 of Fig.15c and Fig.15d) for the 40Hz and 50Hz operation.

The power circuit schematic for generating the multilevel 24-sided polygonal vectors for PWM control of a drive system is in Fig.16a and the 12concentric Multilevel voltage space vector structure form this power circuit is shown in Fig.16c. Here also a single DC link is used for the power circuit and the rest of the power supplies are capacitor fed

H bridges, acting as switched capacitive filters for low order harmonic suppression[36]. In Fig.16a, the Vc1 capacitor voltage is 0.5Vdc, the HB1 capacitor voltage is 0.289Vdc and the HB2 capacitor voltage is 0.1345.The 12 layers of the multilevel 24sided polygonal vector points are switched average vector locations from the HB1 and HB2 three level structures [36]. The schematic of the switched average vector generation for the 24sided polygon is shown in Fig. 16c and the multilevel vector combination from the primary flying capacitor topology and the CHb1 and CHb2 (Fig.16a) are shown graphically in Fg.16.d.

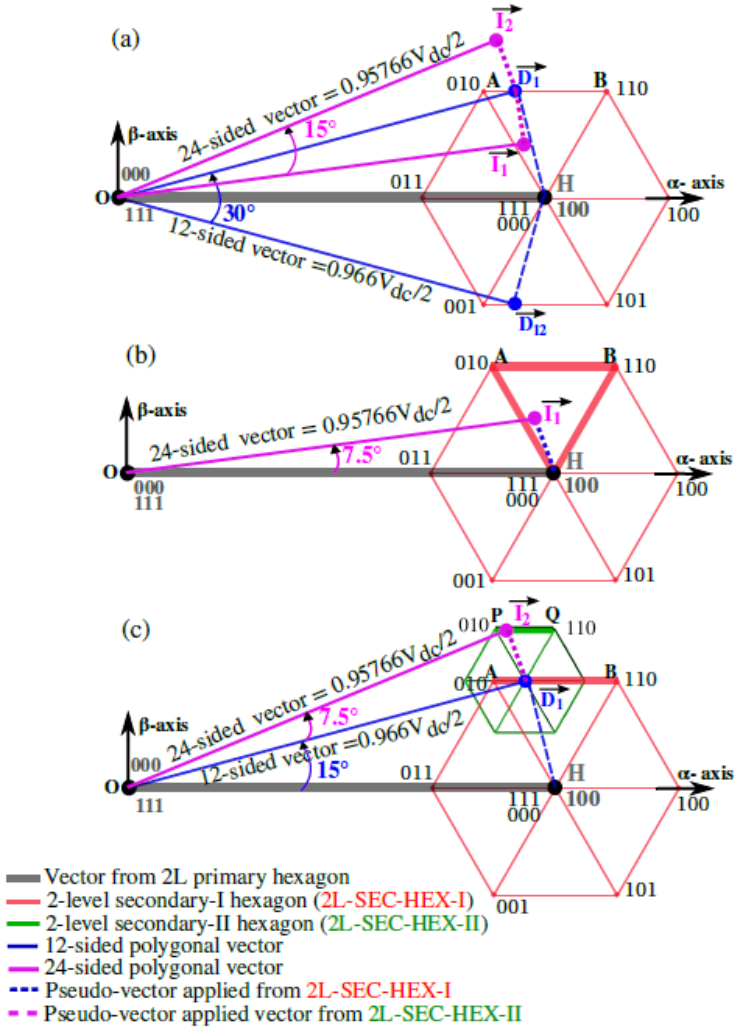


Fig. 16c. Generation of a switched average vector for the 12 sided polygon

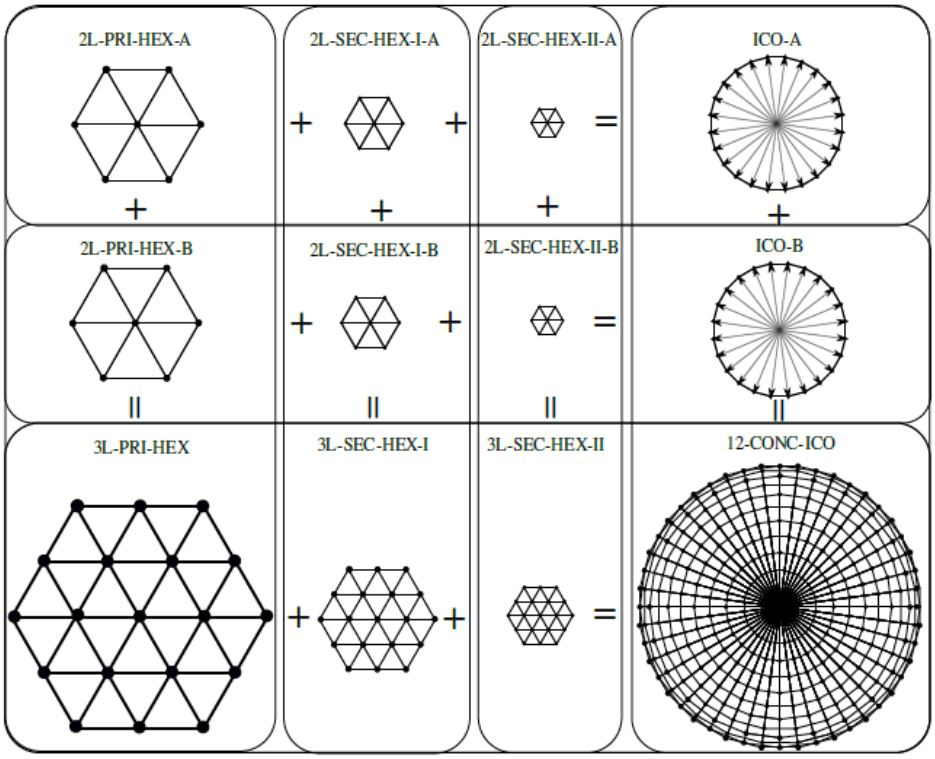
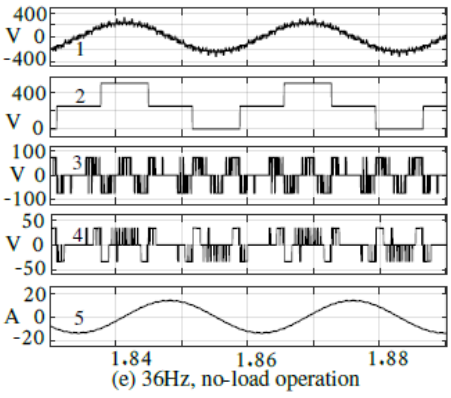
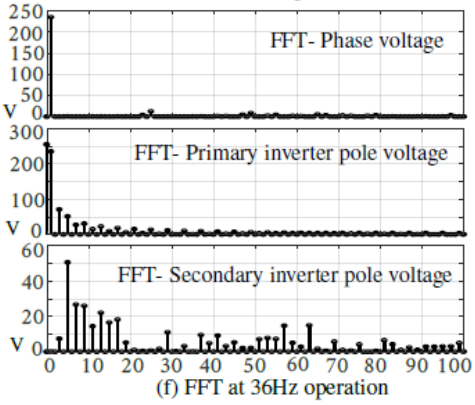


Fig.16d Generation of the 12 concentric multilevel 24 sided polygonal vectors



(e) 36Hz, no-load operation

Fig.16e-36Hz operation (1) Phase voltage, (2) FC inverter pole voltage, (3) HB1 inverter pole voltage, (4) HB2 inverter pole voltage, (5) Phase current (IA)



(f) FFT at 36Hz operation

Fig.16f. Harmonic spectrum at 36 Hz operation

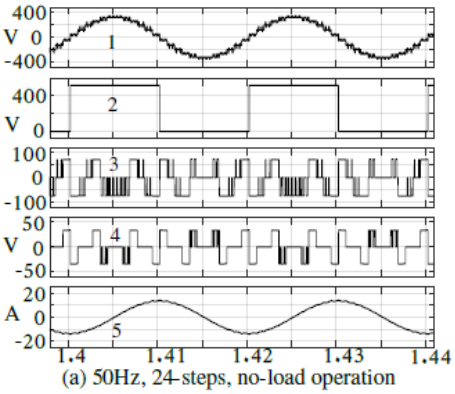


Fig.16g. waveforms at 50Hz operation

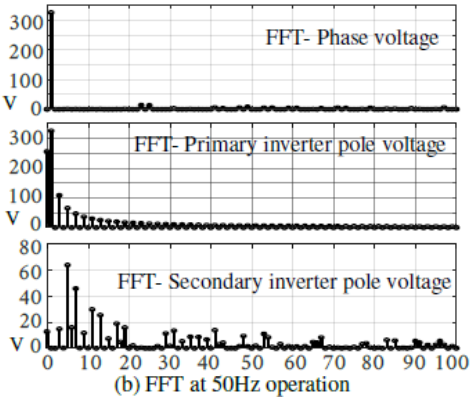


Fig.16h. Harmonic spectrum at 50 Hz operation

Here also it can be noted that the primary Flying capacitor topology works in quasi Square wave mode and most the PWM switchings are transferred to the low voltage H bridges acting as switched harmonic filters and it effectively suppress the low order harmonics up to 19th order. These polygonal schemes can be considered as multilevel inverter schemes with harmonic suppression using low voltage low size switched capacitive filters for variable speed drives applications. Because of the Single DC power supply requirements these topologies can also be driven form directly from the grid using controlled rectifiers with unity power flow control from the grid.

9. References

[1] Philip T. Krein, "Elements of power electronics", Indian edition, Oxford university press.

[2] B. Wu, High power converters and AC drives. IEEE Press, John Wiley and Sons, 2006.

[3] B. K. Bose, Power electronics and motor drives recent progress and perspective, *IEEE Transactions on Industrial Electronics,* vol. 56, no. 2, pp. 581–588, Feb. 2009.

[4] Ned Mohan, Tore M. Undeland, William P. Robbins, "Power Electronics: Converters Applications and Design", John Wiley & Sons, Second Edition, 1995.

[5] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, „Multilevel Converters: An Enabling Technology for High-power Applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[6] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodríguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters", *IEEE Transactions on Industrial Electronics,* vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[7] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug.2002.

[8] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-point Clamped PWM Inverter," *IEEE Transactions on Industry Applications*, pp. 518–523, 1981.
[9] C. Meyer, C. Romaus, and R. W. DeDoncker, Five level neutral-point clamped inverter for a dynamic voltage restorer, *Proc. Conf. Rec. Eur. Conf. Power Electron. Appl.*, vol. 49, no. 5, pp. 11–14, Sept. 2005.
[10] Mohan M. Renge and Hiralal M. Suryawanshi, "Five-Level Diode clamped Inverter to eliminate Common Mode Voltage and Reduced dv/dt in Medium voltage rating Induction Motor Drives, *IEEE Transactions on Power Electronics,*vol. 23, no. 4, pp. 1598–1607 July 2008.
[11] T.A Meynard and H.Foch, "Multilevel choppers for high voltage applications" in Proce. EuropianConference on Power Electronics and applications, 1992, pp. 45–50.
[12] T.A. Meynard, M.Fadel and N.Aouda, " Modeling of Multilevel Converters",*IEEE Transactions on Industrial Electronics*, vol. 44, no. 3, Jun 1997, pp. 356–364.
[13] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, October 2002, pp. 955–964.
[14] T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, „Multicell converters: derived topologies," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, October 2002, pp. 978–987.
[15] Sang-Gil Lee, Dae-Wook Kang, Yo-Han Lee and Dang-Seok Hyun," The Carrier based PWM method for Voltage Balance of Flying Capacitor Multilevel Inverter ", *Conf. Proc. IEEE- PESC-2001,* pp. 126–131.
[16] M.A. Severo Mendes, Z.M. Assis Peixoto, P.F. Seixas, P. Donoso-Garcia and A.M.N. Lima," A space Vector PWM Method for Three-Level Flying-Capacitor Inverters", *Conf. proc. IEEE- PESC-2001*, pp. 182–187.
[17] Brendan Peter McGrathand Donald Grahame Holmes, Natural Capacitor Voltage Balancing for a Flying Capacitor Converter Induction Motor Drive, *IEEE Transactions on Power Electronics,* vol. 24, no. 6, pp. 1554–1561, June 2009.
[18] J. Huang, and K. A. Corzine, Extended operation of flying capacitor multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, January 2006, pp. 140–147.
[19] W. McMurray, "Fast response stepped-wave switching power converter circuit," *US Patent No. 3,581,212*, Filed 31 July 1969 Granted 25 May 1971.
[20] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives", *IEEE Transactions on Industry Applications*, vol. 33, no. 1, pp. 202–208, Jan. 1997.
[21] N. P. Schibli, T. Nguyen, and A. C. Rufer, "A three-phase multilevel converter for high-power induction motors," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, Sept. 1998, pp. 978–986.
[22] R. Gupta, A. Ghosh, A. Joshi, "Switching Characterization of Cascaded Multilevel-Inverter- Controlled Systems," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 3, pp. 1047–1058, March 2008.

[23] Elena Villanueva, Pablo Correa, *Member, IEEE*, José Rodríguez, *Senior Member, IEEE*, and MarioPacas, *Senior Member, IEEE,* "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems", *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4399–4406, November 2009.

[24] Yidan Li and Bin Wu, *Fellow, IEEE,*" A Novel DC Voltage Detection Technique in the CHB\Inverter-Based STATCOM", *IEEE Transactions on Power Delivery*, vol. 23, NO. 3, pp. 1613–1619, July 2008.

[25] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static Var generation, *IEEE Transactions on Industry Applications*, vol. 32, no. 5, Sept./Oct. 1996, pp. 1130–1138.

[26] K. Sivakumar, Anandarup Das, Rijil Ramchand, Chintan Patel, and K. Gopakumar, "A Hybrid multilevel Inverter Topology for an Open-End Winding Induction-Motor Drive Using Two-Level Inverters in Series With a Capacitor- Fed H-Bridge Cell", *IEEE Transactions on Industrial Electronics*, vol. 57, no. 11, November, 2010, pp. 3707–3714.

[27] P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, Jose I. Leon and Leopoldo G. Franquelo, A Five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-bridge," IEEE Transactions on Power Electronics, vol. 27, no. 8, pp. 3505–3512, August 2012.

[28] P. P. Rajeevan, K. Sivakumar, Chintan Patel, K. Gopakumar and Abu- Rub Haitham, "A Nine-level inverter topology for medium voltage induction motor drive with open-end stator winding", *IEEE Trans. Ind. Electron*., 2013, 60, (9), pp. 3627–3636.

[29] P. Roshankumar, Sudharshan Kaarthik, K. Gopakumar, P.P. Rajeevan, Jose I Leon, Leopoldo G Franquelo.,A seventeen-level inverter with a single DC-link for motor drives,"Industrial Electronics Society, IECON 2013 – 39th Annual Conference of the IEEE, pp. 6176–6181, November 2013.

[30] Viju Nair *R*, Arun Rahul S, R. Sudharshan Kaarthik, Abhijit Kshirsagar, K. Gopakumar, „Generation of Higher Number of Voltage Levels by Stacking Inverters of Lower Multilevel Structures With Low Voltage Devices for Drives", *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 52–59, February 2017.

[31] Viju Nair R, Arun Rahul S, Sumit Pramanick, K. Gopakumar, Leopoldo G. Franquelo, "Novel Symmetric Six-Phase Induction Motor Drive Using Stacked Multilevel Inverters With a Single DC Link and Neutral Point Voltage Balancing", *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2663–2670, May 2017.

[32] Mriganka Ghosh Majumder; Rakesh R; Imthias Mohammed; Gopakumar K.; Umanand, Loganathan; Wojciech Jarzyna, „Extending the Linear Modulation Range to Full Base Speed Independent of Load Power Factor for a Multilevel inverter fed IM Drive" ,I*EEE Transactions on Industrial Electronics*, Year: 2019, Early Access Article.

[33] Viju Nair *R*, K Gopakumar, Leopoldo G. Franquelo, "A Very High Resolution Stacked Multilevel Inverter Topology for Adjustable Speed Drives", IEEE Trans. Ind. Electron., vol. 65, no. 3, pp. 2049–2056, Mar. 2018.

[34] Sumit Pramanick; Sudharshan Kaarthik; Najath Abdulazeez, K. Gopakumar; Sheldon Williamson; Kaushik Rajashekara, "A Harmonic Suppression Scheme for Full Speed Range of a Two Level Inverter Fed Induction Motor Drive using Switched Capacitive Filter". *IEEE Transactions on Power Electronics*, Vol. 32, no.3, PP.2064-2071, march. 2017.

[35] Mathews Boby; K.Gopakumar; Arun Rahul; Umanand; Subhashish. Bhattacharya; frede Blaabjerg,"A Low Order Harmonic Elimination Scheme For Induction Motor Drives Using a Multilevel Octadecagonal Space Vector Structure With a Single DC Source"; IEEE Transactions on Power *Electronics*, Volume: 33, Issue: 3, pp. 2430–2437, March 2018.

[36] Krishnaraj R; K Gopakumar; Apurv Kumar Yadav; L. Umanand; Mariusz Malinowski; Wojciech Jarzyna, "A Twelve Concentric Multilevel Twenty-Four Sided Polygonal Voltage Space Vector Structure for Variable Speed Drives" , IEEE Transaction on Power Electronics, Vol. 34, NO.10, Oct 2019, pp. 9906–9915.

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